

CMPE 650: Digital Systems

Course Master

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Lecture

MW 5:30-:6:45 pm

Office hours

After lecture or by appointment

Webpage

<http://www.csee.umbc.edu/~tinoosh/cmpe650/>

Check frequently for class news, handouts, papers, and assignments.

Prerequisites

CMPE 310, CMPE 415

Grading: Letter

50% Homework/minor projects
20% Midterm Exam
25% Final project, demonstration and presentation
5% Classroom participation

Proposed Catalog Course Description

This course covers practical and theoretical aspects necessary to design high-speed and energy efficient digital systems. Emphasis is on design implementation for reconfigurable architectures such as FPGA and non programmable ASIC fabrics and test real systems on an FPGA development board. Topics such as architectures, control, functional units, and circuit topologies for increased performance and reduced circuit size and power dissipation will be discussed.

General Course Description & Objectives

Through this course, students will develop the necessary skills to design systems suitable for numerically intensive processing with an emphasis on FPGA/ASIC implementation flow. Specifically, the course will investigate:

- 1) High-level optimizations such as pipelining, unfolding, and parallel processing
- 2) Key kernel operations and their optimization including arithmetic logics, multipliers, dividers, inversion.
- 3) Modeling of algorithms in Matlab and conversion of Matlab models into fixed-point Verilog blocks
- 4) Algorithms and system implementation on FPGA boards and verification
- 5) Platform implementation issues: hardware vs. software, FPGA vs. ASIC, power, area, throughput, etc.
- 6) FPGA interface with CPU using PCI express, UART and USB

Topical Outline

- II. Processor building blocks
 - A. Quick review of Verilog hardware description language
 - B. Binary number representations
 - C. Types of Adders and Multipliers
 - F. Fixed-input multipliers (optimizations)
 - G. Complex arithmetic hardware
 - H. Memories
- II. Design optimization
 - A. Platform implementation fabrics FPGAs and ASICs
 - B. Verilog synthesis to a gate netlist
 - C. Delay estimation and reduction
 - D. Area estimation and reduction
 - E. Power estimation and reduction
- III. FPGA interface
 - A. Serial UART
 - B. PCI express
 - C. USB
- IV. Projects and system implementation

Textbook

For this course, not a specific reference book is required. Slides will be used in class which covers most of the material. Also for new topics research papers are used as reference.

For basic digital design, FPGA and RTL verilog these books are suggested

Digital Design an Embedded Systems Approach Using VERILOG, Peter J. Ashenden, ISBN: 978-0-12-369527-7, Morgan Kaufmann, 2008.

The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, ISBN: 0750676043

Verilog According to Tom (available on course web page), Tom Chanak

Quick Reference for Verilog HDL (available on course web page), Rajeev Madhavan

Disabilities

Students who are covered under the American Disabilities Act should inform the teacher privately of this fact at the beginning of the class so that appropriate instructional arrangements can be made.

Academic integrity

Cheating in this course will cause you to fail the course. You are encouraged to consult the instructor if you have any questions on homework, projects and/ or exams. By enrolling in this course, each student assumes the responsibilities of an active participant in UMBC's scholarly community in which everyone's academic work and behavior are held to the highest standards of honesty. Cheating, fabrication, plagiarism, and helping others to commit these acts are all forms of academic dishonesty, and they are wrong. Academic misconduct could result in disciplinary action that may include, but is not limited to, suspension or dismissal. Consult the UMBC Student Handbook to read the full Student Academic Conduct Policy.

Late work policy

If assignment is reviewed in class, no credit is possible for late work. If assignment was not reviewed in class, there will be a 1/3 reduction of remaining credit per day (i.e., 100% -> 67%, 44% -> 30% ...).

Regrading policy

Please bring clear grading errors to my attention. Non-obvious grading issues will not be considered due to fairness to all students, and the inherent subjectiveness of grading.

References list

1. B. M. Baas, An Approach to Low-power, High-performance, Fast Fourier Transform Processor Design, Ph.D. thesis, Stanford University, Stanford, CA, USA, 1999
2. Zhengya Zhang, Design of LDPC Decoders for Improved Low Error Rate Performance, Ph.D thesis, University of California Berkeley, CA, USA, 2009
3. Digital Design an Embedded Systems Approach Using VERILOG, Peter J. Ashenden, ISBN: 978-0-12-369527-7, Morgan Kaufmann, 2008.
4. VLSI Digital Signal Processing Systems: Design and Implementation, Keshab K. Parhi, ISBN: 978-0471241867, Wiley, 1999.
5. The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, ISBN: 0750676043
Digital Signal Processing with Field Programmable Gate Arrays, Uwe Meyer-Baese, 3rd Edition, Springer, 2007, ISBN: 978-3540726128.
6. Verilog According to Tom, Tom Chanak
7. Quick Reference for Verilog HDL, Rajeev Madhavan
8. Digital Signal Processing: Principles, Algorithms, and Applications, John G. Proakis and Dimitris K. Manolakis, 4th edition, Prentice Hall, 2006, ISBN: 978-0131873742. [3rd edition also fine]
9. Discrete-Time Signal Processing, Alan V. Oppenheim, Ronald W. Schafer, and John R. Buck, 2nd edition, Prentice Hall, 1999, ISBN: 978-0137549207.