

CMPE 641 - Homework #1

Instructions

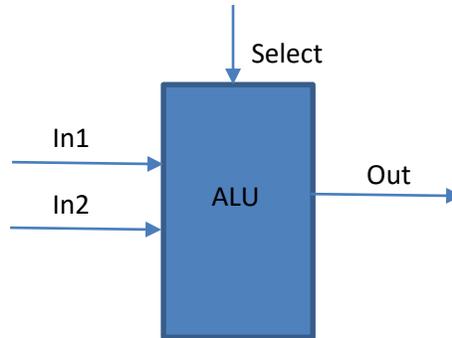
Start assignment as soon as possible. Work individually, but you can ask your classmates for help when you get stuck, with consideration to the **course collaboration policy (please read it in the course website)**. Please send me email if something isn't clear and I will update the assignment.

Notes:

- [15% of points] Clearly state whether your design is fully functional, and state the failing sections if any exist.
- Make sure your design and code are easily readable and understandable (clear and well commented).
- *** Where three '*'s appear in the homework, perform the required test(s) and turn in a printout of either:
 1. a table printed by your verilog testbench module listing all inputs and corresponding outputs

Keep "hardware" modules separate from testing code. Instantiate a copy of your processing module(s) in your testing module (the highest level module) and drive the inputs and check the outputs from there.

Description: Design and Test a 7 function Arithmetic Logic Unit (ALU) written using Verilog and tested with NC-Verilog+NCSim Cadence tool. The ALU is designed as a fully combinational logic, and no clock, flipflop or storage is needed for this design. The input In1 and In2 are each 8-bit signed 2's complement.



Functions that ALU performs upon select signal:

- 1) Add
- 2) Subtract
- 3) Multiply
- 4) Square
- 5) Arithmetic Shift left
- 6) Arithmetic Shift Right
- 7) Negating a Two's complement number (not bitwise negation)

- 1) [10pt] What is the length of Select and Out signals in order to select different functions and provide the output with correct answer?
- 2) [20pt] Draw a block diagram of the ALU design with signal names and necessary logic blocks
- 3) [70pt] Write Verilog for the design and also a testbench for testing the design using ncoverilog+ncsim and examine different input cases with different functions for positive and negative values.