Ferroelectric Field Effect Transistors

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Introduction

- **Ferroelectrics**: dielectric crystals which show a spontaneous electric polarization and the direction of polarization can be reoriented by an external electric field

- In ferroelectric memories, direction of spontaneous polarization is used to store digital bits

Introduction

- Non-volatile electrically switchable data storage devices can be implemented
- Typically implemented as a capacitor consisting of a thin ferroelectric film in between two conductive electrodes

Introduction

- Voltage pulse applied to the cap determines the polarity (“0” or “1”)
- For readout another voltage pulse is applied that determines whether or not polarization switched direction
- Read process is non-destructive

Introduction

- Efforts focused on development of ferroelectric FETs
- Data read out in FeFET in non-destructive
- FeFET has both memory and logic functions
- FeFET is similar to MOSFETs, the gate oxide is a ferroelectric material

Principles of FeFETs

- Ferroelectric memories are based on 1 (MOS) transistor–1 capacitor (1T1C) approach
- Transistor is separated by a thick dielectric layer from ferroelectric cap
- Reliability issues exist in fabrication of 1T1C cell

Principles of FeFETs

- Figure (fig 1) shows the conventional DRAM, 1T1C ferroelectric cell and FeFET

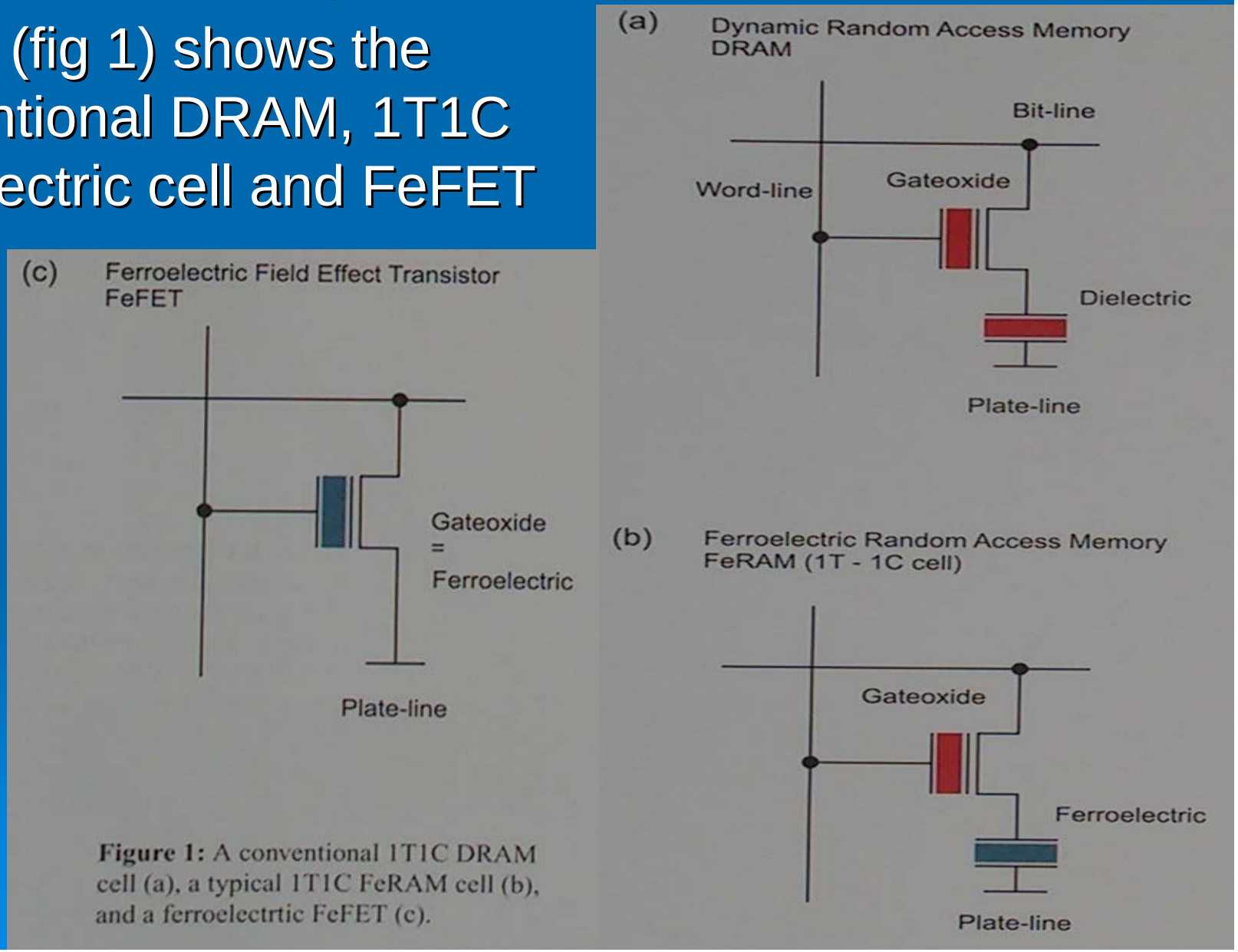


Figure 1: A conventional 1T1C DRAM cell (a), a typical 1T1C FeRAM cell (b), and a ferroelectrtic FeFET (c).

Principles of FeFETs

- Figure (fig 2) shows the layout of a FeFET

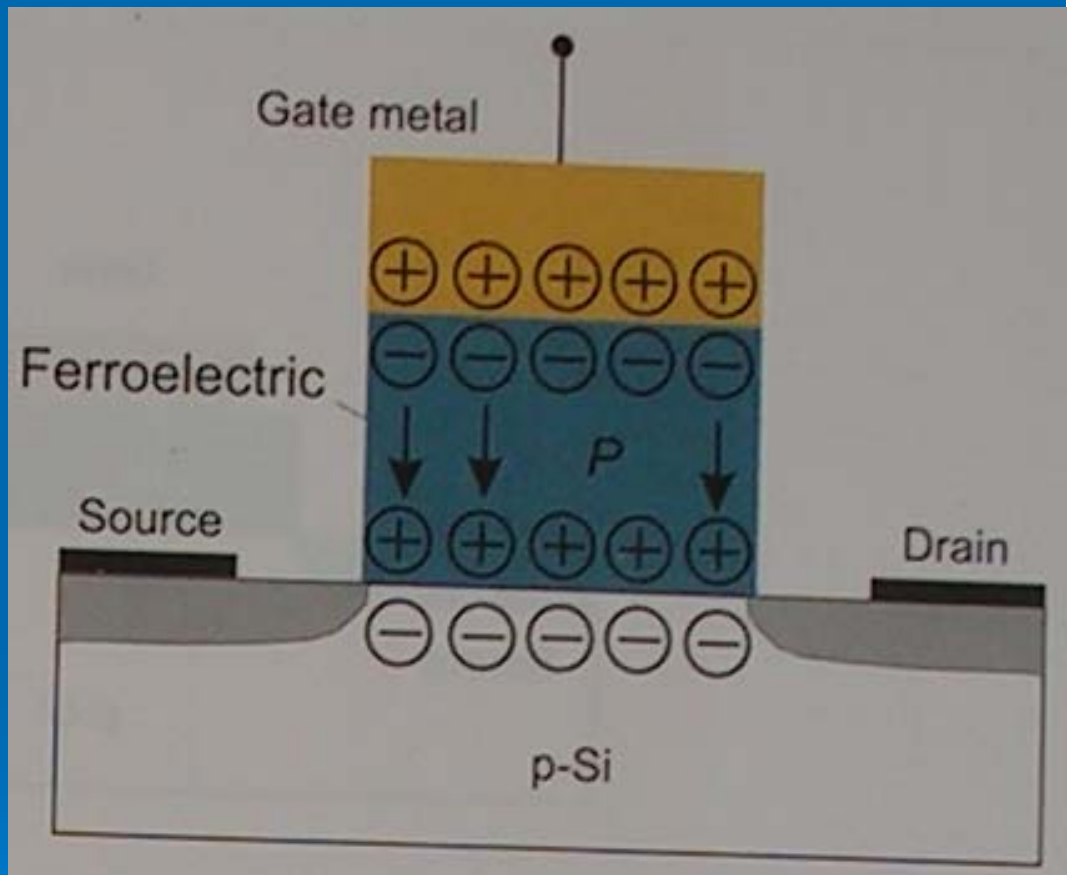
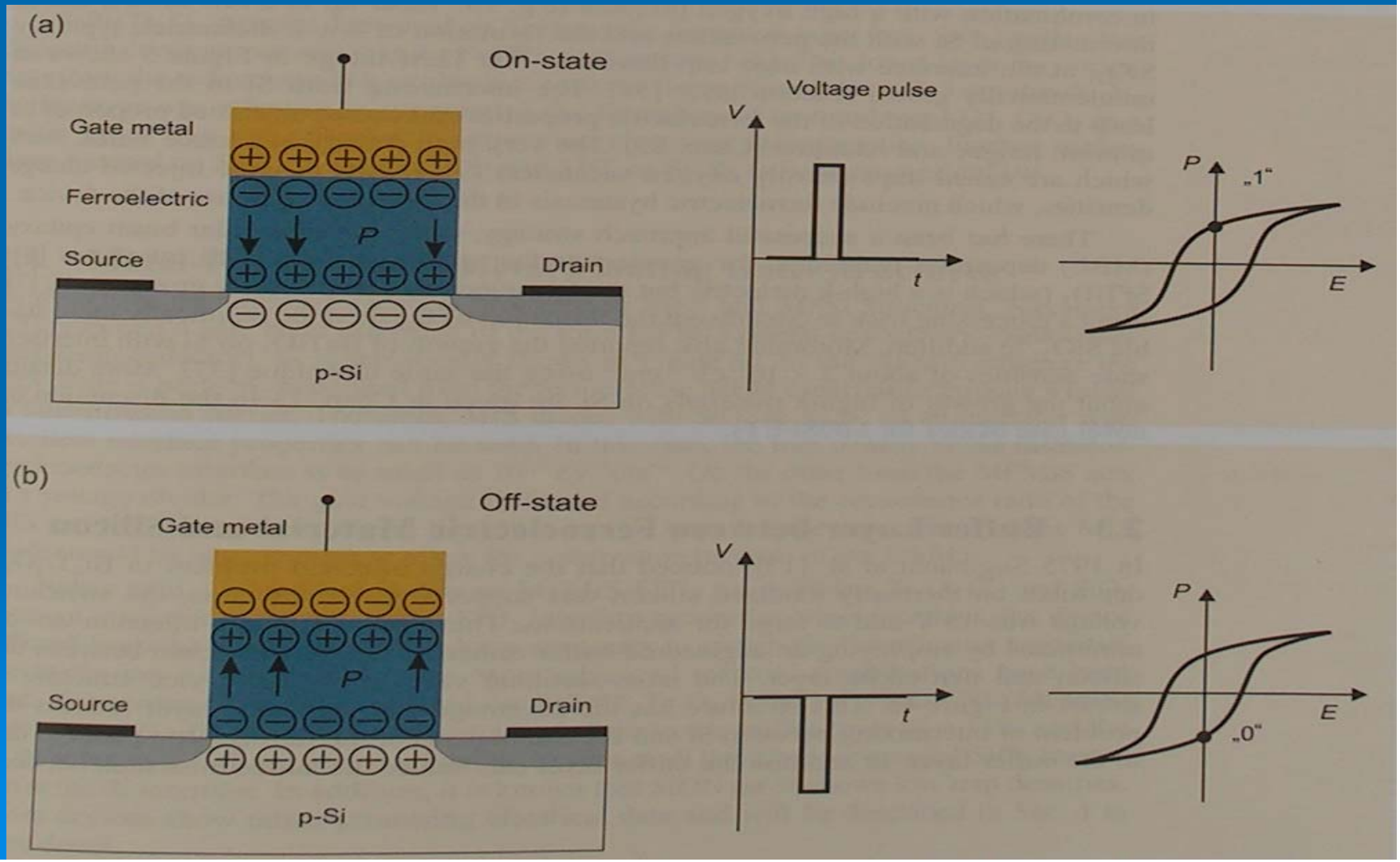


Figure 2: Schematic cross-section of a FeFET. The gate dielectric is a ferroelectric material. As an example a polarization state including surfaces charge layers is shown.

Principles of FeFETs

- Figure (fig 3) shows the charge motion in a FeFET during one cycle of operation



Principles of FeFETs

- Vg>Vc : polarization vector P is directed toward Si
- Accumulation of electrons in channel, on state
- Vg<-Vc : Pr is directed opposite, electrons are depleted
- Non-destructive readout : sense the source drain resistance

➢ FeFET memories: -non-volatile , -non-destructive readout , - compact cell design

Principles of FeFETs

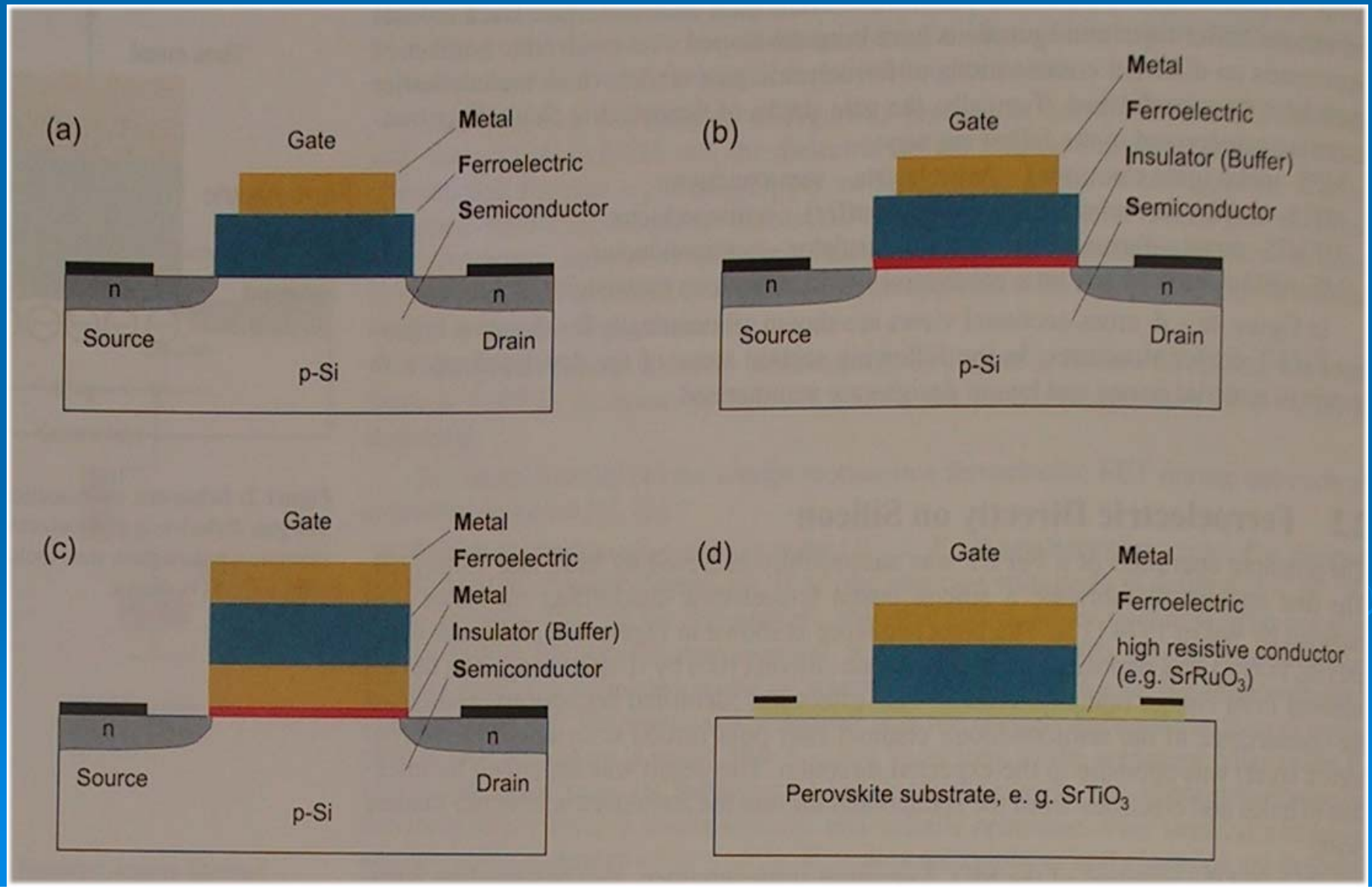
- Design structures for FeFETs and material aspects
  - As seen in the layout of FeFET, a stack of metal-ferroelectric-semiconductor is required for FeFET
  - Challenges in interfacing Si and ferroelectrics:
    - Lattice mismatch must be as small as possible
    - Chemical reactions and intermixing should be minimized
    - Number of interface states should be less than 10^{12} $eV^{-1}cm^{-2}$
    - Formation of low-k dielectrics should be avoided
    - Ferroelectric must form a pinhole free layer

Principles of FeFETs

- Only few **Perovskite** oxides are suitable for growth on silicon
- Alternative gate stack layouts and various buffer layer configurations have been developed:
  - MFS : metal-ferroelectric-semiconductor
  - MFIS: metal-ferroelectric-insulator-semiconductor
  - MFMIS : metal-ferroelectric-metal-insulator-semiconductor
  - MF-ABO3 : ferroelectric on a conductive oxide (no silicon)

Principles of FeFETs

- Figure (fig 4) shows these alternatives



Principles of FeFETs

- Ferroelectric directly on silicon
  - The intermixing from Si to Perovskite leads to the degradation of the ferroelectric properties
- Buffer layer between ferroelectric and silicon
  - The effect of charge injection can be minimized by employing an engineered buffer sandwiched between the silicon and Perovskite layer
  - Buffer layer reduces the problem of intermixing silicon and ferroelectric
  - Gate oxide is comprised of two capacitors in series
  - Buffer layer weakens the electric field across ferroelectric

Principles of FeFETs

- Metal-ferroelectric-metal gate structures
  - MFMIS structure reduces the intermixing problems
  - However, it acts as a voltage divider
  - Gate voltage is divided according to capacitance ratio of the MIS and MFM
  - Capacitance of MIS diode should be large enough to allow the polarization reversal of MFM
  - Relatively large voltage necessary to switch the ferroelectric capacitor (in case of SiO_2 insulator)

Principles of FeFETs

- Meta-Ferroelectric on a conductive oxide
  - Source-drain channel is replaced by a conductive oxide
  - These have similar growth conditions as ferroelectrics
  - The aim is to modulate conductivity of the conductive oxide by the polarization of ferroelectric

Electrical characterization of FeFETs

- For MFIS gate structure the drain current in linear regime is given by:

$$I_D = -(W/L)\mu_h[P^* + C(V_{GS} - V_T)]V_{SD}$$

$$P^* = PC_B/(C_B + C_{Fe})$$

L : gate length , W : gate width , μ_h : effective hole mobility

P : polarization of ferroelectric , C : gate capacitance per unit area

- The drain conductance and transconductance are given by:

$$g_D = -(W/L)\mu_h[P^* + C(V_{GS} - V_T)]$$

$$g_m = -(W/L)\mu_h C V_{SD}$$

Electrical characterization of FeFETs

- Hence, source-drain current shows two characteristics for two different polarizations (+/-P)

- **MFIS structures**

BLT ((Bi,La)4Ti3O12) is an important candidate

C-V characteristics for Pt/BLT (100 nm)/si3N4 (3 nm)/Si structure is shown in the figure (fig 7)

- Memory window is 1.2 v for c-axis oriented film

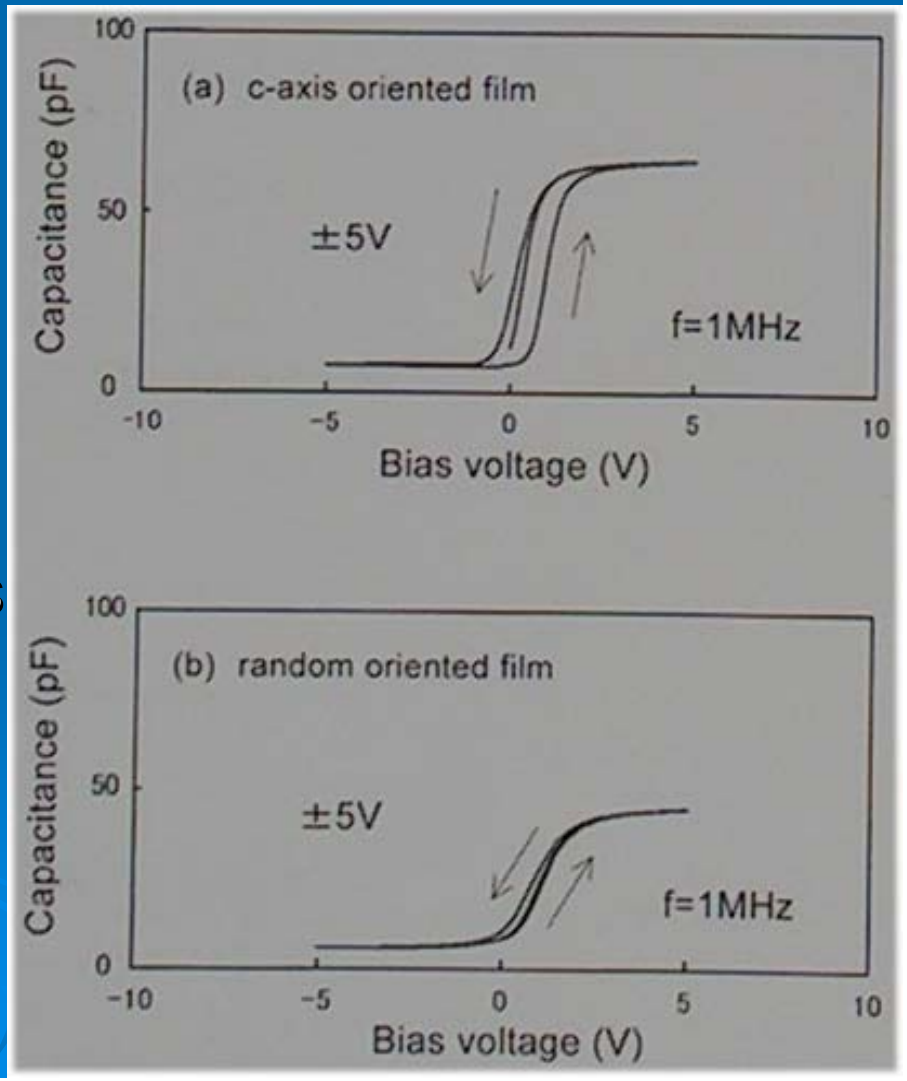


Figure 7: C-V characteristics of Pt/BLT/Si_3N_4/n-type Si diodes. (a) c-axis-oriented film (b) randomly oriented film [38].

Electrical characterization of FeFETs

Figure (fig 8) shows that retention time can be long enough

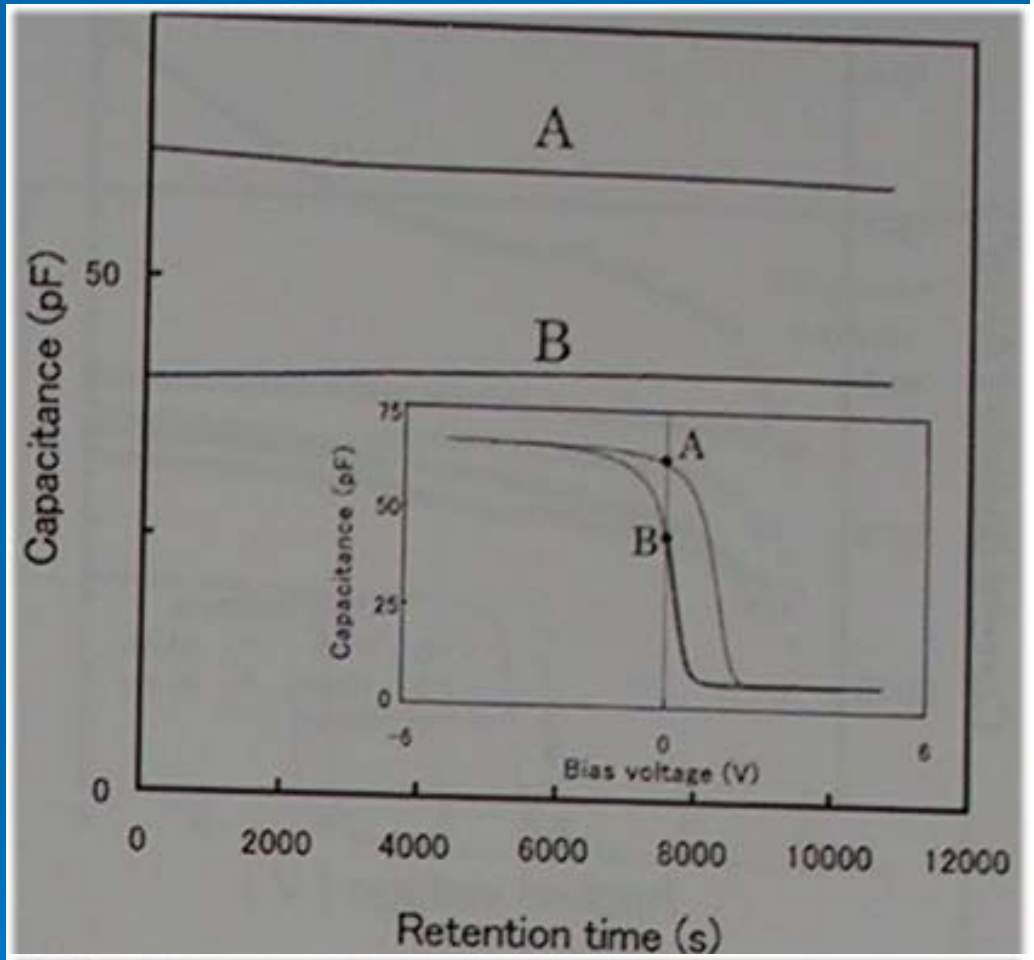


Figure 8: Variation of the zero bias capacitance of a Pt/100 nm-$Bi_{3.25}La_{0.75}Ti_3$ = 12/3 nm-Si_3N_4 Si MFIS diode with time at 300 K. The inset shows the C-V curve [38].

Electrical characterization of FeFETs

- MFMIS structures
  - Figure (fig 14) shows the structure

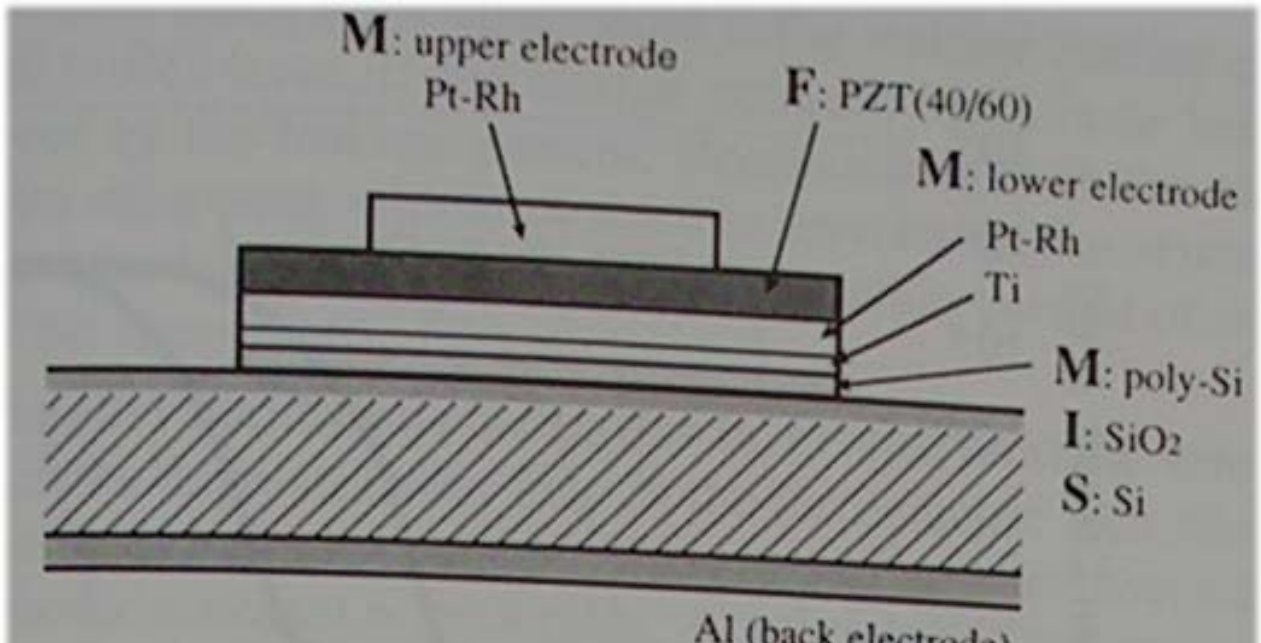


Figure 14: Schematic cross-section of a Ti/Pt-Rh(**M**)/$PbZr_xTi_{1-x}O_3$(**F**)/Pt-RhTi(**M**) MFMIS sample [36].

Electrical characterization of FeFETs

- C-V curve is displayed in figure (fig 15)
- Source-drain current versus gate voltage is shown in the figure (fig 16)

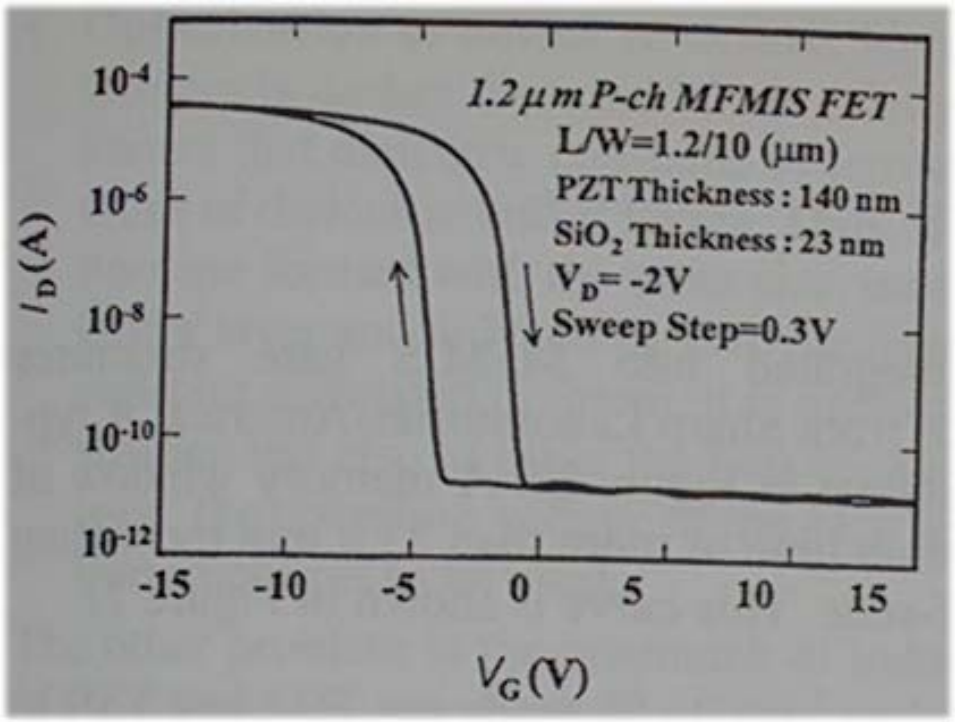


Figure 16: I_{d}-V_{gs} characteristics of 1.2 μm p-channel MFMIS using an Ir/IrO2/$PbZr_xTi_{1-x}O_3$/ Ir/IrO2/poly-Si/SiO_2/Si gate stack.[23].

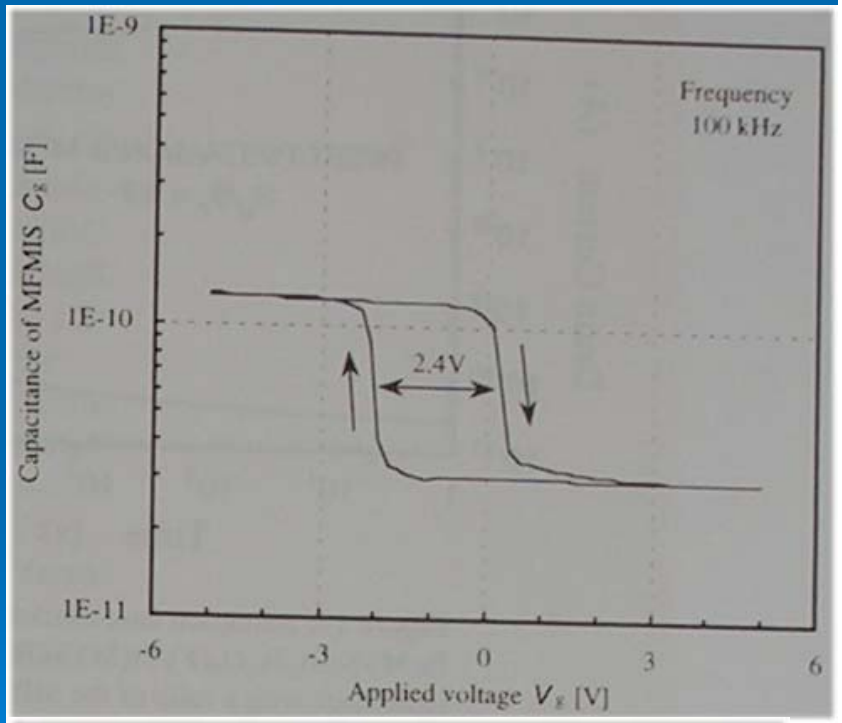


Figure 15: Metal-Insulator-Semiconductor C-V measurement. The structure was: Ti/Pt-Rh(**M**)/$PbZr_xTi_{1-x}O_3$(**F**)/Pt-RhTi(**M**). The sweep frequency was 100 kHz with an amplitude of +/- 5 V [36].

Electrical characterization of FeFETs

- Optimization of FeFETs
  - Short retention times originates from the fact that dielectric capacitor is connected in series with ferroelectric capacitor
    - Under short circuit condition, direction of electric field in ferroelectric is opposite of the polarization
  - Leakage current between ferroelectric and buffer, removes the charges, hence the stored data cannot be readout

Electrical characterization of FeFETs

- To minimize depolarization field, buffer layer capacitance must be as large as possible

- Leakage current must be reduced
- It is necessary to make the ferroelectric film smaller and thicker than the buffer, otherwise, most of the external voltage will be applied to buffer layer (because dielectric constant of ferroelectric constant is much large than the buffer)
- Too thick ferroelectric makes the operation voltage too high

Electrical characterization of FeFETs

- Cell designs and device modeling for FeFETs
  - A 1T-2C cell is proposed to face short retention times of FeFETs (fig 24, 25)

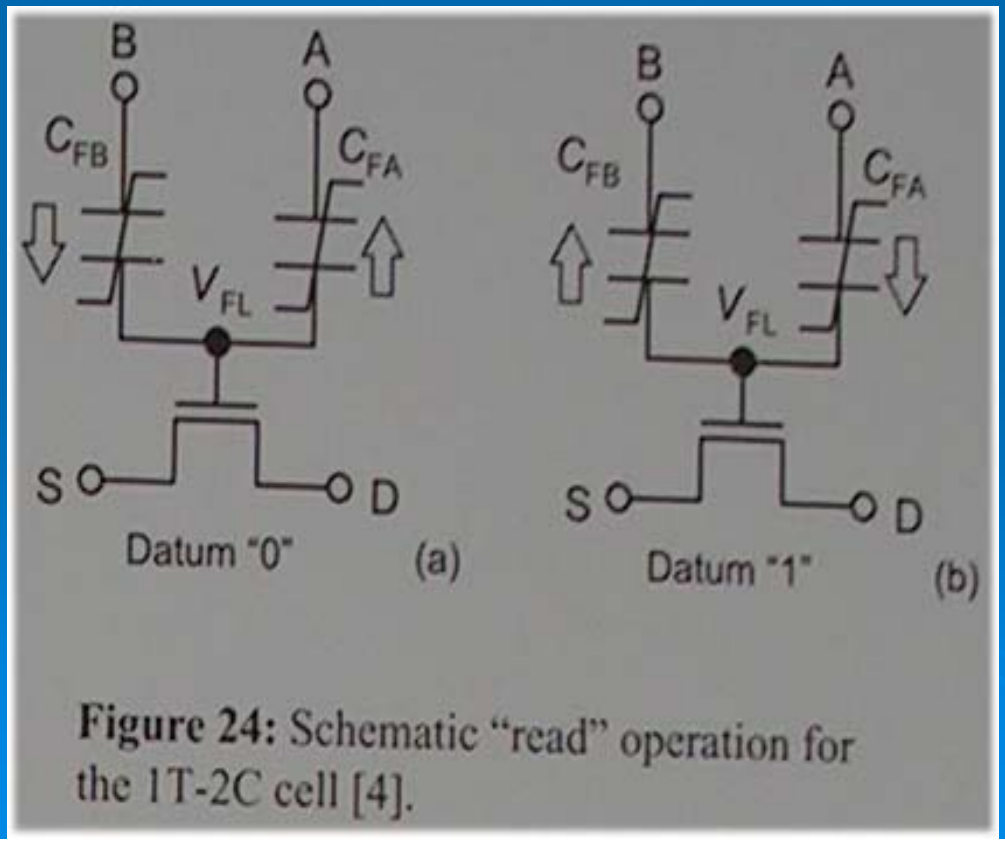


Figure 24: Schematic "read" operation for the 1T-2C cell [4].