Assignment I: Standard Cell Library Design

You will modify and add cells to the standard cell library provided on the Oklahoma State University's VLSI Computer Architecture Research site. The process that we will use is TSMC 0.18 using SCMOS rules, with a lambda of 0.1. The NCSU CDK provides the technology file for this process. We will used a modified technology file that contains some extra rules, which is provided in the class locker. Part I will involve Layouts and Abstract Generation and Part II will involve library characterization. We will characterize the library with typical, slow and fast process parameters. The main tools you will be using: Cadence Virtuoso, Abstract Generator, ADE/Spectre/SpectreS and Encounter Library Characterizer.

Part I: Layout and Abstract Generation

The X1 sized inverter in the library uses a NOMS device with W/L ratio of 1.0/0.2. We will use a smaller inverter using a NMOS device with half the width as our X1 cell. Rename the existing cells in the library to reflect this i.e. X1 becomes X2, X2 becomes X4 and so on. Modify the existing cells to remove as much metal2 as possible from the standard cells. Ideally you should be able to design the cells with only poly and metal1. Add the following cells to the existing library, remember you will need to rename the existing cells and make new cells with the lower drive strength.

AND2 (X1)
AOI21 (X1)
AOI22 (X1)
BUF (X1, X8)
CLKBUF (X1, X2, X4)
DFFNEG (X1)
DFFPOS (X1)
DFFSR (X1)
DFFNSR (X1)
INV (X1)
LATCHN (X1)
MUX2 (X1)
NAND2 (X1)
NAND3 (X1)
NOR2 (X1)
NOR3 (X1)
OAI21 (X1)
OAI22 (X1)
OR2 (X1)
SDFFNEG (X1, X2)
SDFFPOS (X1, X2)
SDFFSR (X1, X2)
SDFFNSR (X1)
TBUF (X1)
TBUFI (X1, X2, X4)
TIEHI

TIELO
XNOR2 (X1)
XOR (X1)
REG1R1W (X1)
REG2R1W (X1)

Create the layouts, perform simulations to verify functionality and generate the abstract view for each of the cells. We will discuss the steps involved and each of the tools in detail during class.

Part II: Library Characterization

Perform library characterization using the Encounter Library Characterizer. We will limit the maximum output slew to 3.0 ns. Use 10%-90% points for slew calculations and 50% points for delay calculations. You will characterize the library at three different design corners, the transistor models will be provided in the class locker. You will use 7 index values for input slew, 7 for output capacitance and 3 for clock related timing checks. Generate the .lib, verilog simulations files and the documentation html file for your standard cells. Verify the output files and add the missing information e.g. scan cell definitions.

Report:

Write a detailed report explaining your standard cell library e.g. cell dimension, power and ground rail dimensions, routing grids, special cells, test features, metal2 usage, options used for abstract, setup file used for library characterization. Include the characterization data generated by the library characterizer. The report should serve as a datasheet for your library as well as a guide to add other cells to the library.