

Allegro PCB Design

Allegro PCB Design is a circuit board layout tool that accepts a layout-compatible circuit netlist (ex. from Capture CIS) and generates output layout files that are suitable for PCB fabrication. This tutorial is the second part of the PCB project tutorial. Before starting with PCB Design, you must have a completed schematic with no errors. The beginning of this tutorial runs through how to create a netlist from your schematic. Simple steps in producing PCB layout involve importing the netlist, placing components, routing and generating output files and reports.

Capture CIS Tutorial (Continued)

Inserting Footprints

For every part used in the schematic in Design Entry CIS, there must be an accompanying footprint. The footprints are provided in a zipped folder on the CMPE 310 homepage. The footprints should be in a folder in the same directory as the schematic DSN file. There is also a PCB Footprints PDF with the footprint names corresponding to the parts. For each part, left click and then right click on the part. Select Edit Properties. Under PCB Footprint, insert the footprint name from the PDF and then hit Apply to save.

| | |
|------------------------------|-----------------------------|
| | A |
| | + SCHEMATIC1 : PAGE1 |
| Color | Default |
| Designator | |
| Graphic | 8086MIN.Normal |
| ID | |
| Implementation | |
| Implementation Path | |
| Implementation Type | <none> |
| Location X-Coordinate | 540 |
| Location Y-Coordinate | 80 |
| Name | INS102 |
| Part Reference | U1 |
| PCB Footprint | DIP10040W600L2025 |
| Power Pins Visible | <input type="checkbox"/> |
| Primitive | DEFAULT |
| Reference | U1 |
| Source Library | C:\CADENCE\SPB_16.0 ... |
| Source Package | 8086MIN |
| Source Part | 8086MIN.Normal |
| Value | 8086MIN |

Figure 1: Inserting footprints from Design Entry CIS

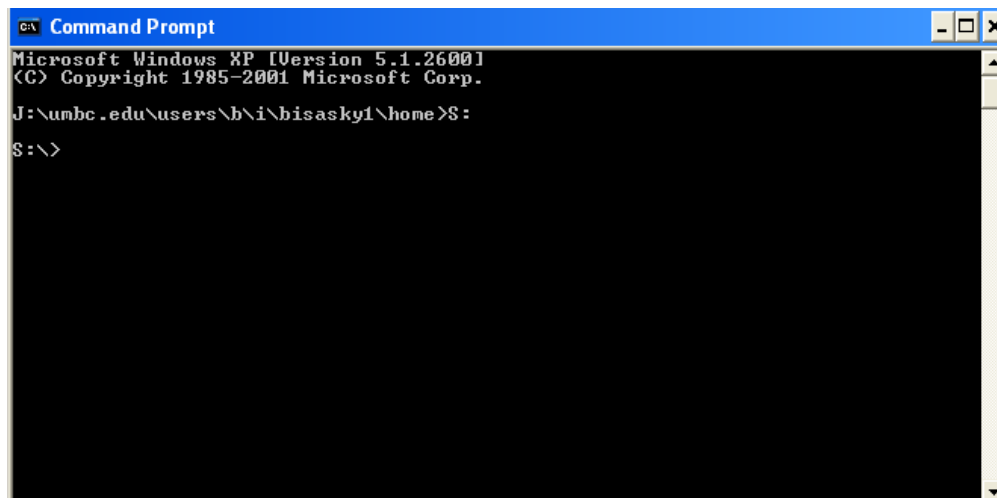
Creating the Netlist

The next step is to generate the netlist from the schematic created in Design Entry CIS and then import the netlist to the PCB Editor. We are generating the netlist using the command line in Windows XP.

First, go to the folder containing your schematic. Create a folder titled "Allegro". Additionally, verify that your footprints are in a folder titled "Footprint".

Open the command prompt: **Start -> All Programs -> Accessories -> Command Prompt**

Type "S:" into the command prompt to move to the S drive.



```
Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

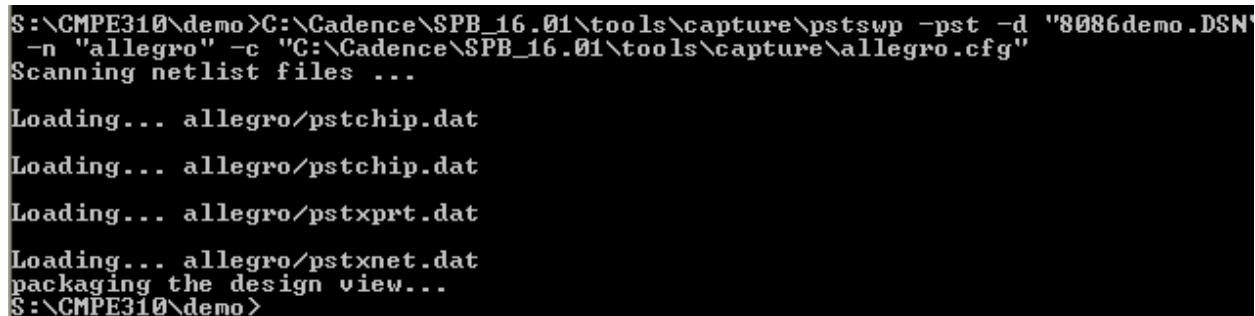
J:\umbc.edu\users\b\i\bisasky1\home>S:
S:\>
```

Figure 2: Change directory to "S:\" drive

Move to the folder containing your schematic: i.e. "cd 310/finalproj/"

Now at your project's directory, type the following command (one line):

```
C:\Cadence\SPB_16.01\tools\capture\pstswp -pst -d "demo.DSN" -n "allegro" -c
"C:\Cadence\SPB_16.01\tools\capture\allegro.cfg"
```



```
S:\CMPE310\demo>C:\Cadence\SPB_16.01\tools\capture\pstswp -pst -d "8086demo.DSN"
-n "allegro" -c "C:\Cadence\SPB_16.01\tools\capture\allegro.cfg"
Scanning netlist files ...
Loading... allegro/pstchip.dat
Loading... allegro/pstchip.dat
Loading... allegro/pstxprt.dat
Loading... allegro/pstxnet.dat
packaging the design view...
S:\CMPE310\demo>
```

Figure 3: Running netlist

Allegro PCB Editor

Creating a board

Open PCB Editor: **Start ->All Programs ->Cadence SPB 16.01 -> PCB Editor -> Allegro PCB Design XL**

Create a new board by going to **File -> New**

Browse to the S Drive directory of choice (preferably the same location as your schematic), insert a Drawing Name and set the Drawing Type to Board.

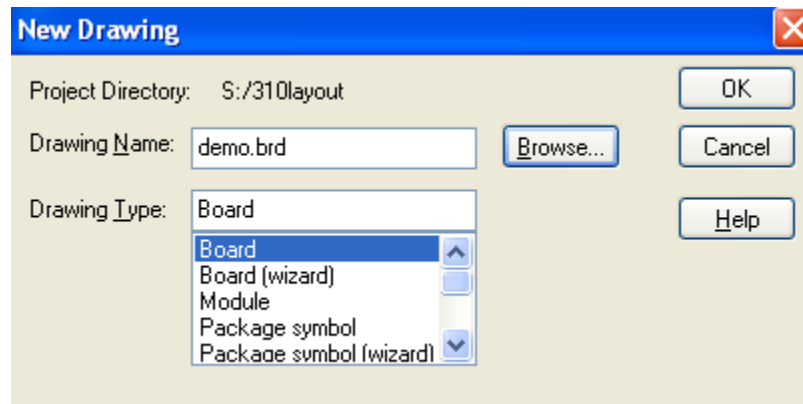


Figure 4: Creating a new board

Importing the Netlist

Before importing the netlist, you must set the directory path to your footprint folder.

Setup -> User Preferences -> Categories: Design Paths -> psmpath (...)

Add the directory path to your footprint folder. Then click OK to confirm.

Repeat the same step for the padstacks.

Setup -> User Preferences -> Categories: Design Paths -> padpath (...)

Add the directory path to your padstack folder (most likely the same location as the footprint folder). Then click OK to confirm.

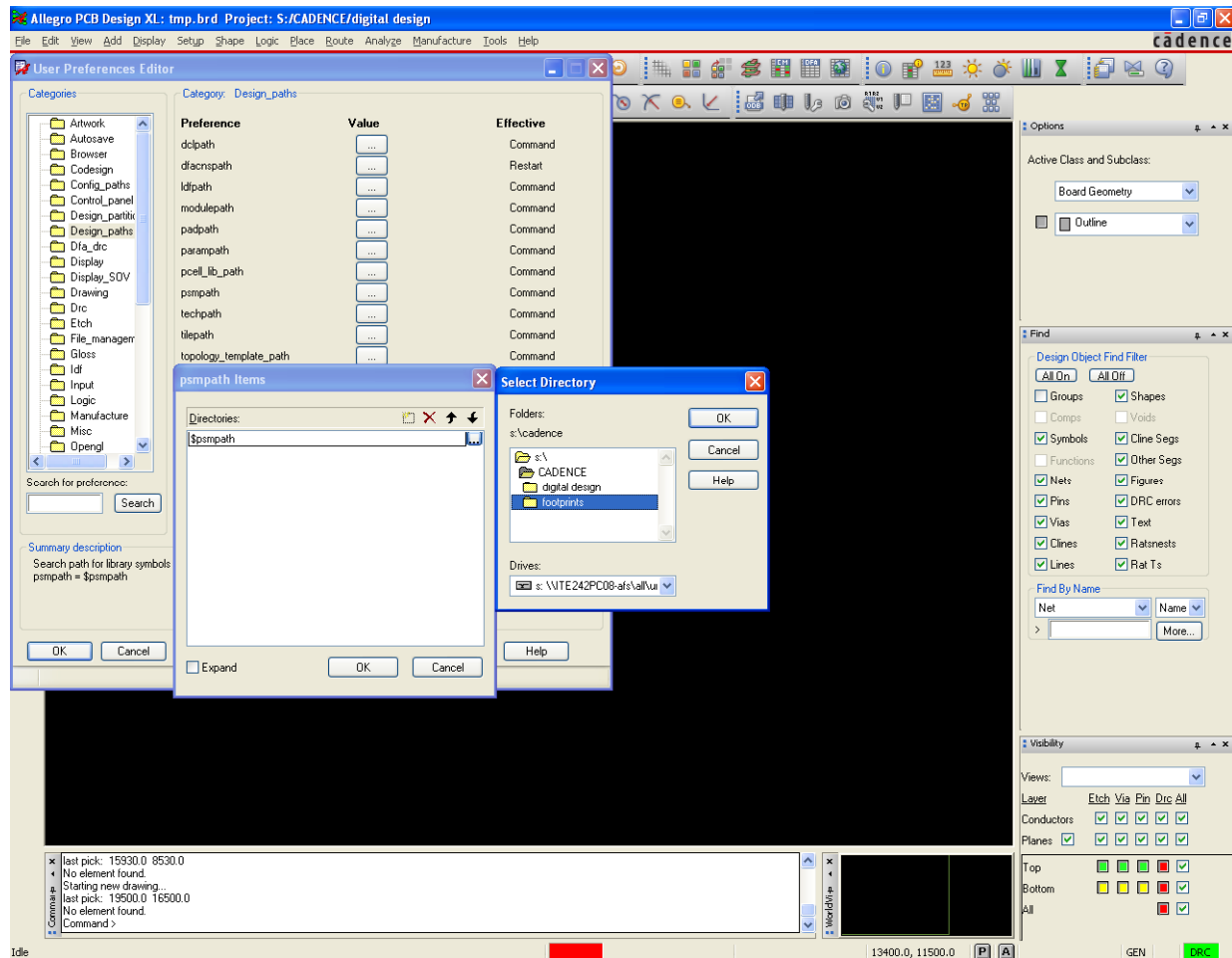


Figure 5: Changing footprint path

To import the schematics from Design Entry CIS:

File -> Import -> Logic

For Import Design Type, set to Design entry CIS (Capture). Place changed component to Always. Leave everything else unchecked. For Import Directory, set to the allegro folder (i.e. S:/CMPE310/finalproj/allegro).

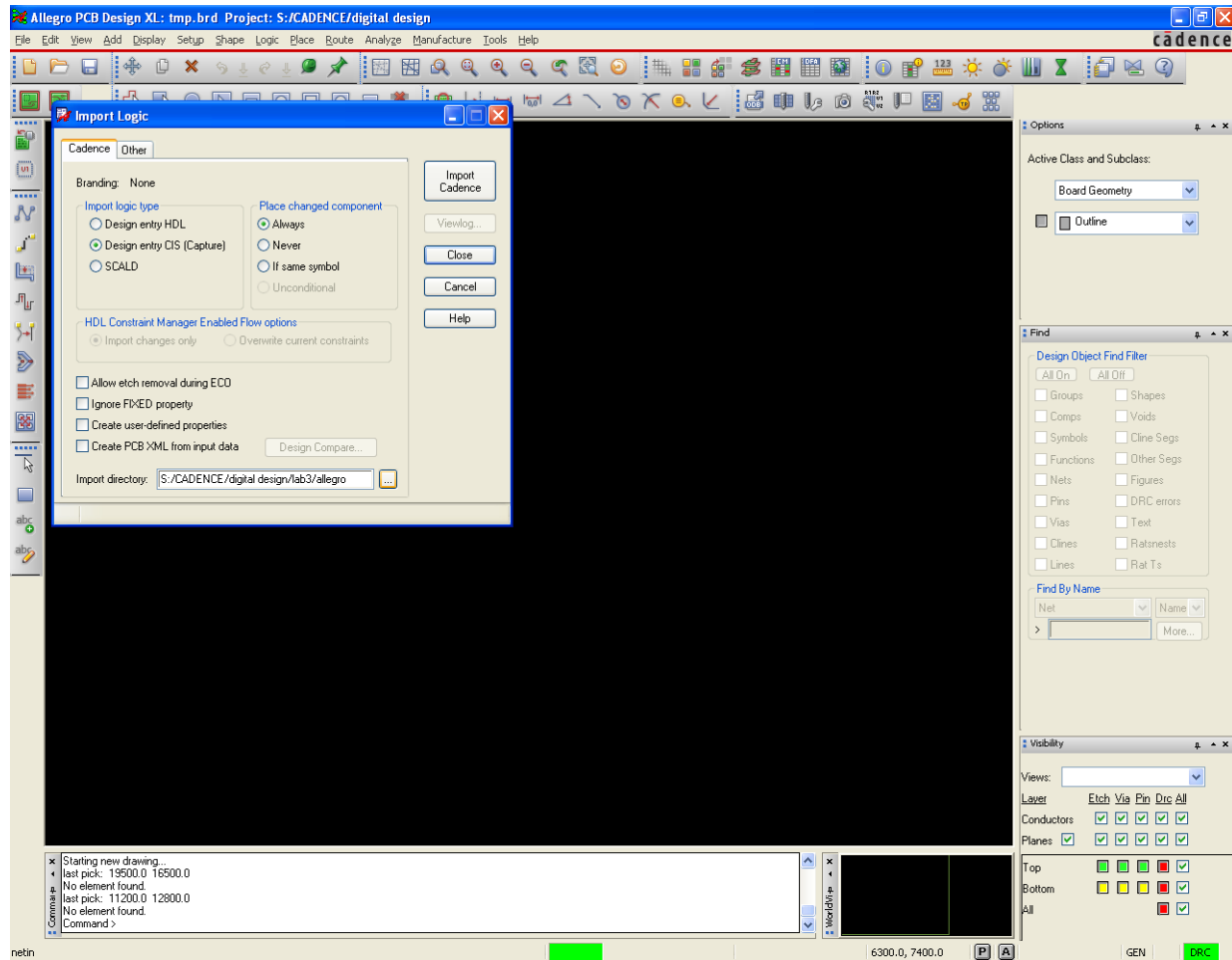


Figure 6: Import Logic—“Import directory” is the allegro folder found within the project directory

Click Import Cadence. If no output file opens then your netlist was successfully imported with no errors or warnings. If there are errors, correct your schematic in Design Entry CIS and re-netlist/import logic until no errors occur.

Setting up the Board Layers

For the project, we are using a four layer board. The default is two layers so to change the number, go to **Setup -> Cross-Section**. Right click between the Top and Bottom layers to add four layers. Follow **Figure 7** to add the GND and Power layers and appropriately set the Type to Dielectric or Plane. The Layout Cross Section should match the figure.

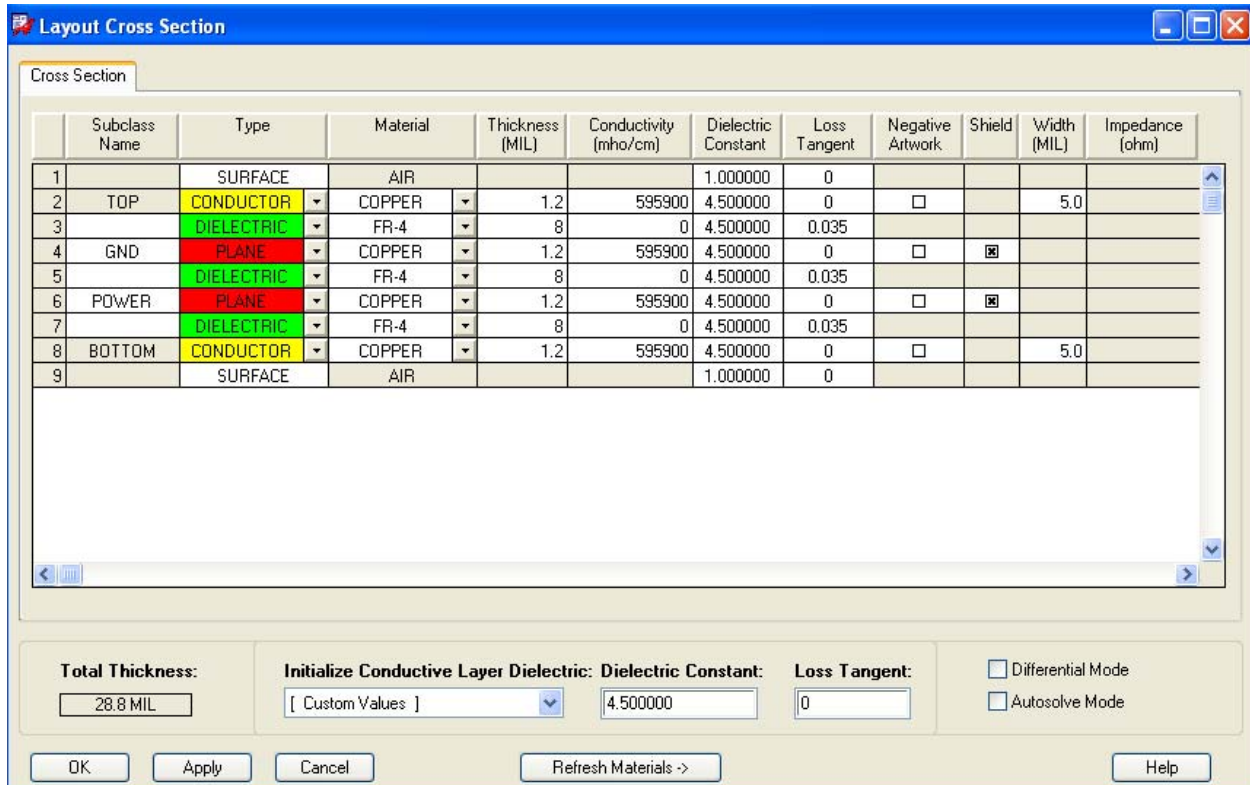


Figure 7: Setting the number of layers to four

Allegro PCB Editor settings must be changed to support the board size needed for the project. To increase the available board size, go to **Setup -> Design Parameters** which opens the Design Parameters Editor. Select the Design tab and change the Extents to the following:

- Left X: -500
- Lower Y: -500
- Width: 15000
- Height 15000

The units are in Mils where 1000 Mils = 1 inch. All of the other settings should match those in **Figure 8**.

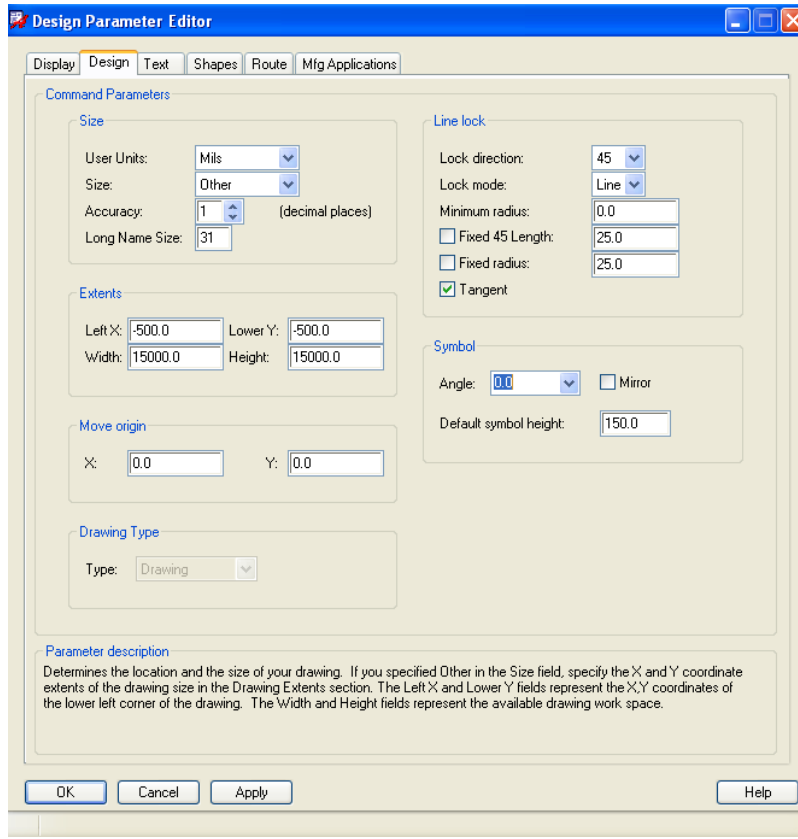


Figure 8: Adjusting the Design Parameters Editor to support the required board size

Creating the Board Outline

To create the board outline: **Setup -> Outlines -> Board Outline**

Under Command Operations, select Create and under Create Options, set to Place Rectangle.

Set the Board Edge Clearance to 100.0 MIL. Set Wdt and Hgt both to 12000 MIL (12 inches).

Do not click OK.

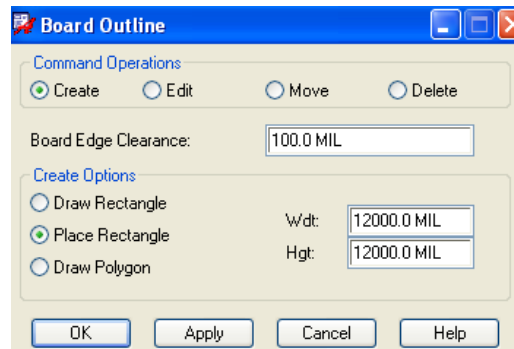


Figure 9: Creating the Board Outline

Place board outline in the lower left hand corner of the window by left clicking. Again, **do not** click on OK.

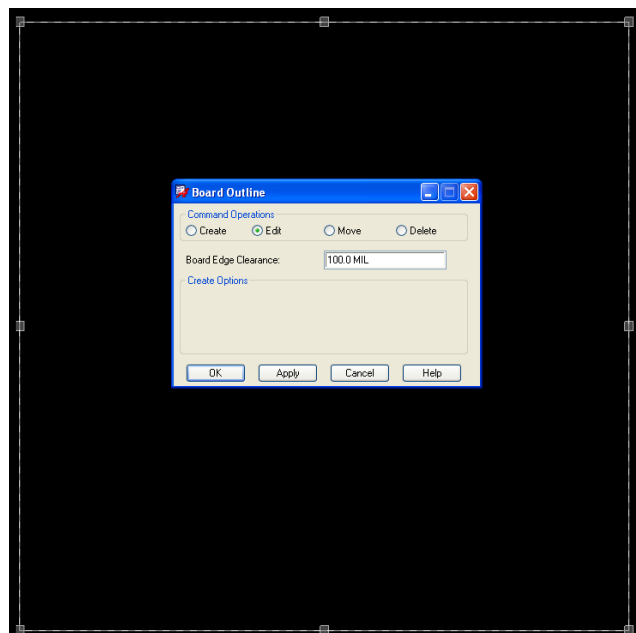
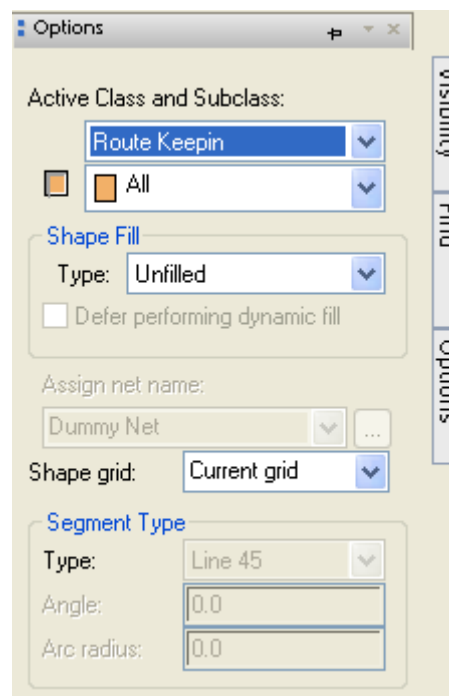


Figure 10: Placing the board outline

Still do not click OK, but place the first rectangle in the window by going to **Shape -> Rectangular**. A purple rectangle should appear within the board outline.

Go to Options (on the upper right hand corner of the window), select the Active Class as Route Keepin and set the Subclass as All. The rectangle color should change from purple to a tannish red.

**Figure 11: Changing the rectangle class**

Now create another rectangle overlapping the previous rectangle by again going to **Shape -> Rectangular**. Click in the top left corner of the tannish red rectangle and then click on the lower right corner of the tannish red rectangle. Then right click and select Done to place the new rectangle.

The two rectangles now overlap each other.

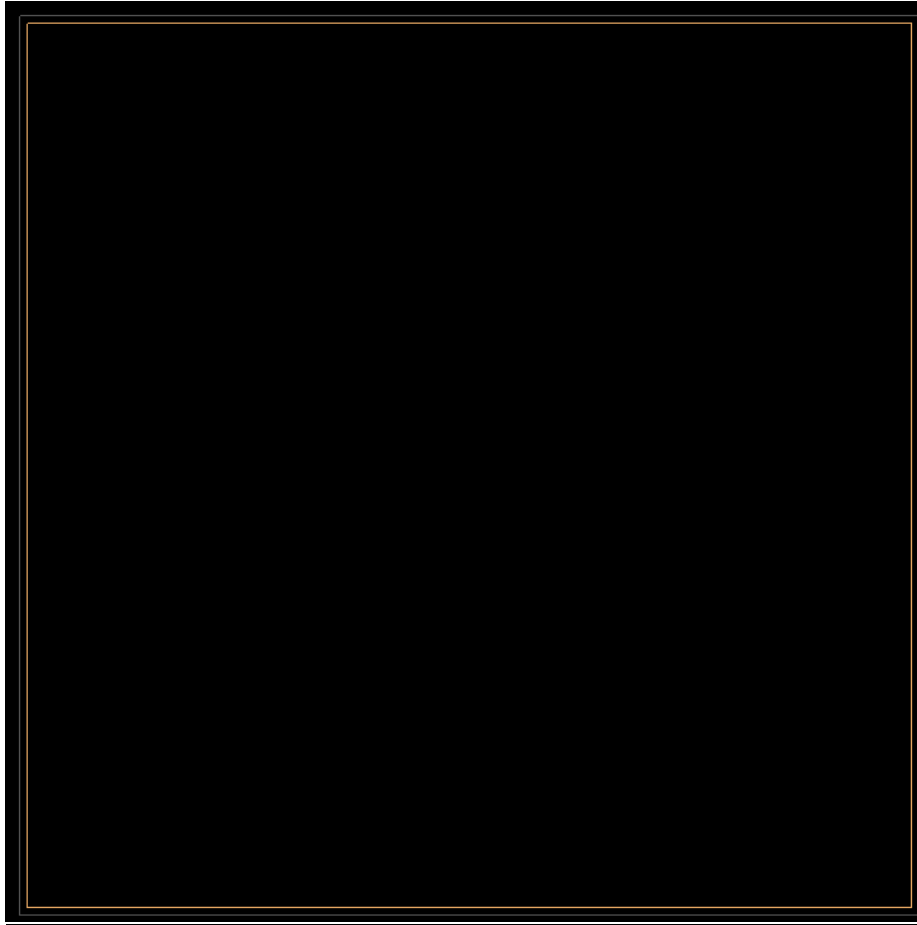


Figure 12: Adding the second rectangle

Placing Parts

To place the parts from the schematic, go to **Place -> Manually**. The parts will be in the Placement menu listed by their part names (i.e. U1, U2, R1, etc). Checking the box of one of the parts will allow you to place that part onto the board. Do this for all of the parts. When completed, click on OK.

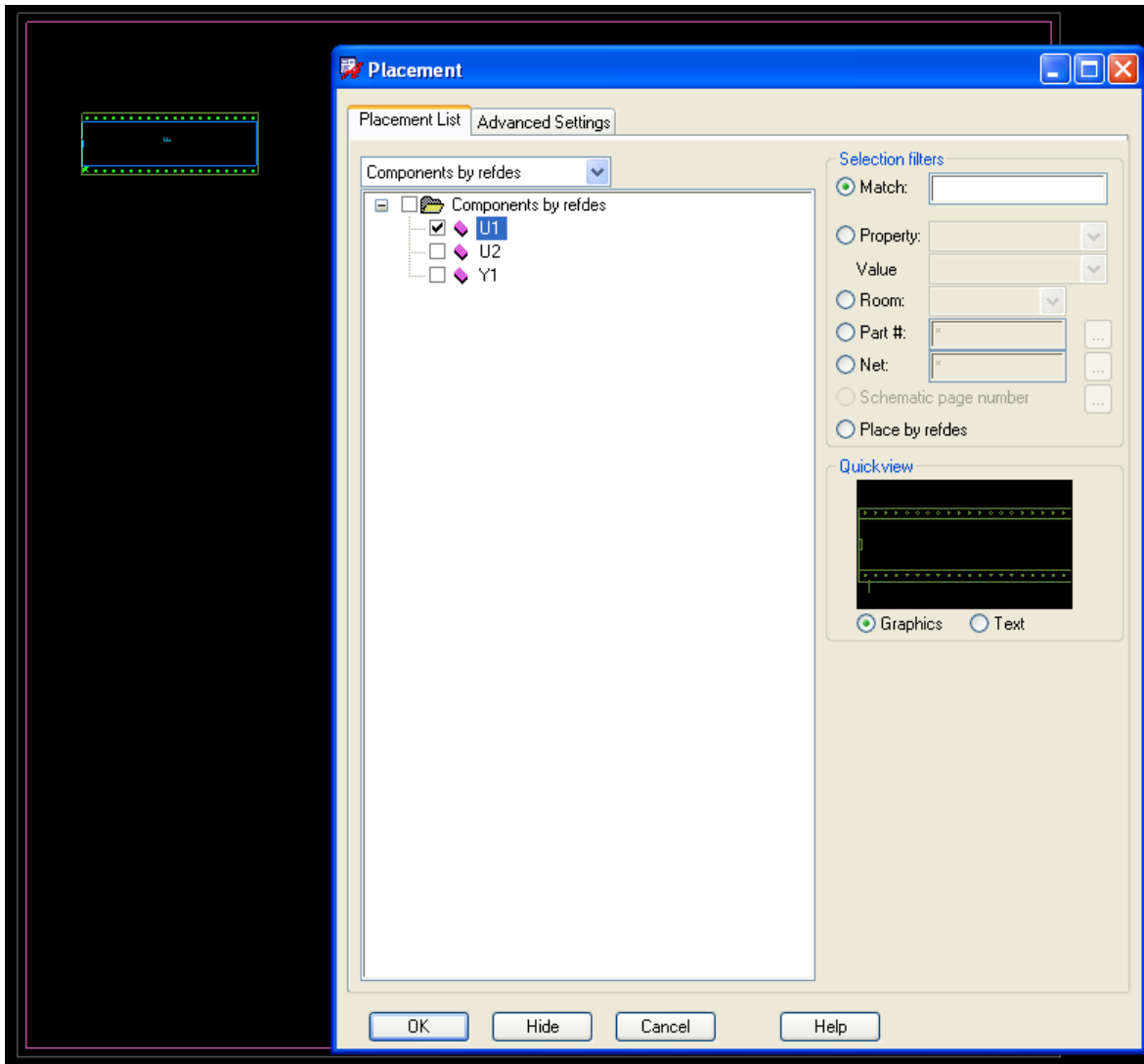


Figure 13: Placing parts – Placing the 8086

Routing

First, set the width of the wires: **Setup -> Constraints -> Constraint Manager**

Select the Physical tab, select Physical Constraint Set, and then All Layers. Under Type PCS with Objects DEFAULT, set the width under column Line Width Min to 20.0 and set the width under Neck Min Width to 20.0.

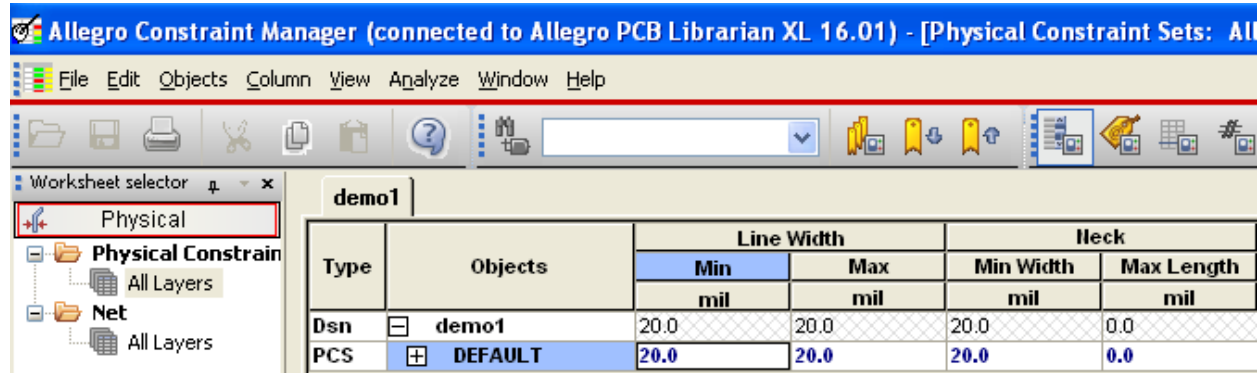


Figure 14: Changing the wire widths

To route the connections, go to **Route -> Route Automatic**. Leave the settings to the default and select Route. In the final project, this step can take upwards of 30 minutes.

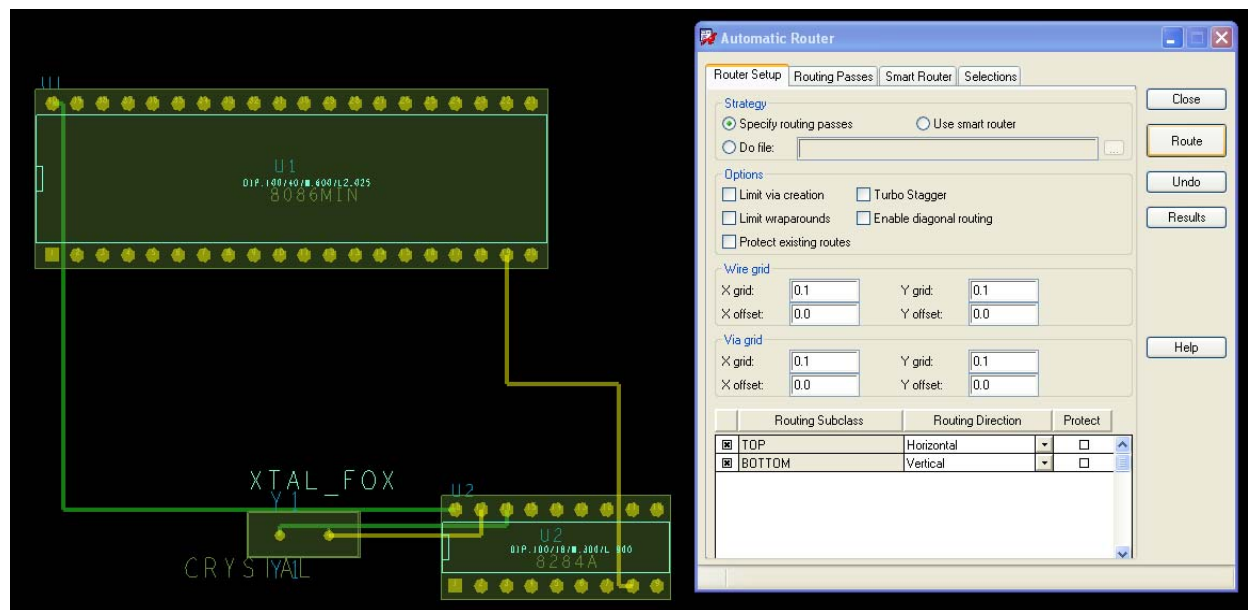


Figure 15: Auto routing the parts

