

On-Chip Impulse Response Generation for Analog and Mixed-Signal Testing

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Abstract

A technique for testing analog and mixed-signal linear circuit components based on their impulse response (IR) signatures is presented in this paper. A simple DFT structure is proposed to enable the on-chip generation of the impulse response signatures from the corresponding step responses of the circuit components. The proposed technique circumvents the need to apply pseudorandom patterns and perform complex on-chip cross-correlation for IR generation. A set of post processing steps based on cross/auto-correlation are proposed to efficiently compare IR signatures. A statistical approach based on linear regression and outlier analysis is used for defect screening. A continuous-time active state variable filter benchmark circuit is used as the Device-Under-Test as a means of validating this technique. The detection sensitivity for shorting and open resistive faults across various defect severity levels is analyzed. The detection results are compared and shown to be superior to a typical specification based test.

1.0 Introduction

The proliferating microelectronics industry is challenged by the requisite of innovative test technologies to provide high quality, low cost defect detection methodologies. Traditionally testing of analog circuits is performed by measuring each parameter in their performance parameter set and comparing it against the tolerance bounds specified by the circuit designer. Devices that fall inside the tolerance limits are classified as defect-free and those that fall outside are identified as outliers or defective. This type of test method is generally referred to as *functional* or *specification based testing*. Due to the elaborate nature of performance specifications, a typical functional test requires generation and application of stimuli with diverse characteristics. This is followed by the measurement of the Device-Under-Test's (DUT) response and in most cases a complicated post processing of the measured response, in order to extract these performance parameters. The above requirements dictate the use of expensive test, measurement and analysis instrumentation. Furthermore, the post processing increases the test time significantly, rendering functional testing uneconomical.

Analog device testing inherently faces a greater set of challenges as compared to digital circuit testing. This can be attributed to: 1) the continuous nature of the signal values with respect to time which makes the output signal sensitive to the entire transfer curve of the system, 2) analog circuit operation is highly dependent on the interaction between various circuit components, parameters, operating

conditions etc. and 3) the analog chips or subsystems are more I/O limited than digital ICs. Furthermore, the variability of functional characteristics of analog circuits due to component variations and fluctuations in processing parameters complicates the testing problem. Several techniques for mixed-signal and analog circuit testing have been proposed in the last decade. Significant work has been done in reducing the test cost and complexity using Built-in Self-Test (BIST) and novel DFT techniques, presented in [3][7] and [10]. Impulse response based testing [4], [9] and [10] has been identified as a powerful technique for testing linear analog circuit components and DFT structures have been proposed for the same.

Impulse Response, henceforth referred to as *IR*, can be used to characterize dynamic behavior of any linear, time-invariant (LTI) system (or circuit). The IR of a linear system provides information on how the system responds to each frequency component in the input impulse, provided that the spectral bandwidth of the input impulse exceeds that of the system. Since IR provides functional information of a linear circuit component, any testing technique that uses the IR to characterize defect-free and defective devices is essentially functional in nature. However, since IR is used to implicitly infer the performance parameters for device classification instead of directly measuring them, such test methods can be called *implicit* functional tests [10]. Due to this characteristic there is a significant advantage in using IR for testing linear analog components because fault modeling of analog circuits is a complex problem.

Several methods exist for obtaining the IR of a LTI system. These include impulse and step response tests, sinusoidal oscillation tests, deconvolution based frequency domain techniques, and cross-correlation methods. Amongst the above mentioned methods, the cross-correlation method has been extensively used for more than the past four decades to characterize and test linear systems including analog circuits. This method was proposed in the early sixties [1-2]. Since then, similar concepts have been used in [4], [8], [9] and [10] for analog and mixed-signal circuit testing. The main advantage of the cross-correlation method lies in the fact that the IR of a LTI system can be obtained under normal operation of the system. Although this method greatly alleviates the need for generating complex test stimuli, the DFT structures, composed of LFSRs,

correlation circuits, and/or data converters, required to enable such test methods are complicated.

In this paper we present a simple scheme, to test analog and mixed-signal linear circuits based on their IR signatures derived from the corresponding step responses. We propose a DFT structure to enable on-chip generation of IR signatures using a pulse generator and differentiator circuit constructed using a flip-flop and a single operational-amplifier (opamp) respectively. There are several benefits of the proposed technique and DFT structure.

- It requires a single flip-flop to generate the pulse stimulus unlike LFSRs required to generate close approximations to white noise in cross-correlation based techniques.
- It needs a simple differentiator circuit based on a single opamp thereby eliminating the need for large cross-correlation circuits for IR generation. In the proposed technique, output of the differentiator directly provides the IR signature of the DUT. On the other hand, the cross-correlation based methods require a special circuit to perform on-chip cross-correlation operations just to obtain the IR signature.
- This technique does not require application of long pseudo-random logic sequences to the DUT required in the case of cross-correlation based methods, thereby significantly reducing the test time.

Once the IR signatures are obtained, they need to be analyzed using some signal processing technique to quantitatively compare the DUT's IR with the defect-free IR. This step is imperative to any technique based on investigation of IR signatures for defect detection. In our recent work [5], we proposed a technique to compare IR signatures for characterizing power supply grids of digital ICs. A similar technique, that improves on this method, is used in this paper to effectively compare the IR of a DUT with the *reference IR (RIR)*, which is obtained from a golden device. Two waveforms are generated; the first, by autocorrelation of the RIR and the second, by cross-correlation of the RIR with the DUT's IR. The *xy*-locations of the *peaks* in these waveforms are used for defect screening. Here, the *peak xy*-location corresponds to the *x* and *y* coordinates, where *y* is the peak value of the auto/cross-correlation curve and *x* is the time instance at which this peak is attained. The efficacy of this test method is demonstrated on an *active universal or state-variable filter* in the presence of wide range of device and component variations.

The cross-correlation operation mentioned above can be performed as a part of data post processing, as our technique uses it only for defect screening and not for generation of IR signatures. However, the inclusion of an on-chip cross-correlation circuit can transform the proposed DFT structure into a BIST solution for testing analog/mixed-signal circuits.

The rest of this paper is organized as follows. Section

2.0 presents some background on properties relating step and impulse response. Section 3.0 presents the proposed test methodology and the DFT structure. Section 4.0 presents the experimental design. Section 5.0 describes the fault-model and simulation setup. Section 6.0 provides details of the experimental results and observations. Section 7.0 presents our conclusions.

2.0 Impulse Response and Step Response

Any linear time invariant (LTI) system can be completely characterized by its *Impulse Response (IR)* function denoted as $h(t)$. Where the impulse response $h(t)$, is the output of the system to an impulse function, $\delta(t)$, as shown in Figure 1. The significance of IR lies in the fact that it con-

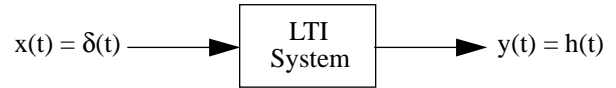


Fig. 1. Impulse response of a LTI system

tains complete information about the system, that is, how it will react to any possible signal. We can construct the response of the system to an arbitrary input signal as a sum of suitably delayed and scaled impulse responses. This process is called *convolution* and is mathematically described using Equation 1. Here, $x(t)$ is the input signal, $y(t)$ is the output signal and $h(t)$ is the IR. The steady-state frequency

$$\begin{aligned}
 y(t) &= h(t) \otimes x(t) && \text{Eq. 1.} \\
 &= \int_{-\infty}^{\infty} h(\tau)x(t-\tau)d\tau \\
 &= \int_{-\infty}^{\infty} h(t-\tau)x(\tau)d\tau
 \end{aligned}$$

response, $H(j\omega)$, of a system can be obtained by performing Fourier transform on its impulse response.

Theoretically, the IR of a LTI system can be derived by stimulating it with an impulse input. However, generating a practically acceptable impulse function is somewhat challenging and its generation on-chip further aggravates the problem. Due to the finite energy of a impulse-like signal, the response of a circuit to such a signal may be significantly corrupted by noise. We use a simple differentiation property of LTI systems to derive the impulse response from the *Step Response* function denoted as $s(t)$. Here, step response, $s(t)$, is the output of the system to a step input function, $u(t)$. The differentiation property states that if $y(t)$ is the output of a LTI system to input $x(t)$ then the time-derivative of $x(t)$ generates an output which is also a time-derivative of $y(t)$. This is described by Equation 2 and can be generalized for any linear operation in lieu of differentiation. Based on the above property we can derive the impulse response of a LTI system by computing the time

$$x(t) \rightarrow y(t)$$

$$\frac{d}{dt}x(t) \rightarrow \frac{d}{dt}y(t) \quad \text{Eq. 2.}$$

where \rightarrow denotes the transformation due to the LTI system

$$\delta(t) = \frac{d}{dt}u(t) \Rightarrow h(t) = \frac{d}{dt}s(t) \quad \text{Eq. 3.}$$

derivative of its step response as given in Equation 3 and shown in Figure 2.

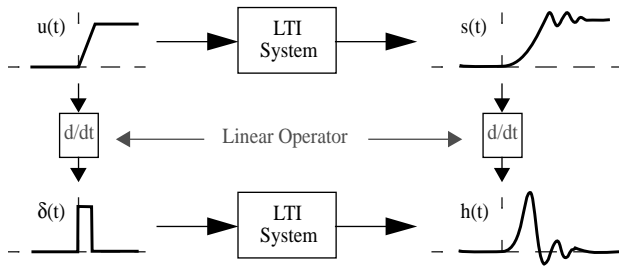


Fig. 2. Generation of impulse response from the step response of a LTI system.

The rise time and the slope of the step input required to generate the step response corresponds to the width and the peak amplitude, respectively, of the impulse-like input that would produce the IR. The rise-time of the step input generated by the pulse generator must be small enough to produce a true step response. In most practical cases this is decided experimentally by applying step inputs of decreasing rise times and the output is rendered as the step response when its shape no longer changes with the change in input rise time. However, in some cases a rule of thumb given by Equation 4 may be used to derive these properties of the stimulus. Here, T_{rise} represents the rise time of input step and T_{IR} represents the *impulse response time* of the linear system. Alternatively, this can also be stated in frequency domain, in which case the input signal must excite the system with all the frequencies that it can respond to, as given by the frequency response of the system. Therefore the spectral bandwidth of the input stimulus (BW_s) must be higher than that of the system (BW_{IR}) as shown in the equation.

$$T_{rise} \leq 10T_{IR} \quad \text{or} \quad BW_s \leq 10BW_{IR} \quad \text{Eq. 4.}$$

This method of impulse response generation has several benefits. The step input with the desired rise time is easy to generate on-chip in today's technologies using a sequential element such as a flip-flop. For mixed signal

designs this is trivial due to the presence of on-chip digital logic. Also as mentioned in Section 1.0, long pseudo random logic sequences need not be used thus reducing the test time and such stimulus generation saves a lot of area compared to ones that use LFSRs.

3.0 Test Methodology and DFT Structure

Figure 3 shows the block diagram of the DFT circuit required to test the DUT. The proposed test methodology

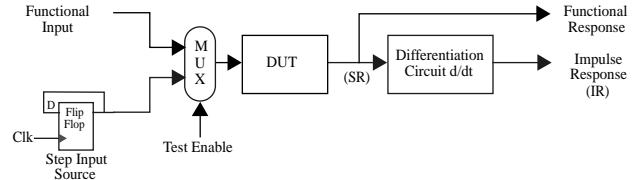


Fig. 3. Block diagram of the DFT circuitry around the DUT illustrating the test methodology.

requires the DUT to be stimulated by a step input signal. This step input may be applied externally through primary inputs (PIs) or by the on-chip digital logic. The on-chip digital logic may be provided as a part of the DFT structure or a digital portion of pre-existing functional logic may be used. The output of the DUT to the step input, which corresponds to its step response, is applied to the differentiation circuit which generates the impulse response of DUT. We use the impulse response of the nominal defect free circuit (golden device) as the reference, referred to as *RIR*. The presence of a defect or variations in circuit and/or device parameters may cause the impulse response of a DUT to vary from the reference signal in terms of amplitude and/or shape characteristics. A defect detection criteria, therefore, must have a means of quantifying the heterogeneity between the two IR waveforms in terms of their shape characteristics. This is achieved using a technique that is based on cross-correlation and auto-correlation operations.

Cross-correlation of two waveforms results into a third waveform whose amplitude indicates the degree of similarity between the two waveforms. Also, the location of its peak indicates the time-shift required in the second signal to obtain the maximum match with the first signal. This is mathematically expressed by Equation 5, where $r_{xy}[i]$ rep-

$$r_{xy}[i] = x[i] \oplus y[i] \quad \text{Eq. 5.}$$

$$= \sum_{j=0}^{M-1} x[j]y[j-i] = \sum_{j=0}^{N-1} y[j]x[j-i]$$

$$r_{xx}[i] = x[i] \oplus x[i] = \sum_{j=0}^{M-1} x[j]x[j-i]$$

resents cross-correlation of two waveforms $x[i]$ and $y[i]$.

When $x[i]$ and $y[i]$ are identical, the operation is termed as *autocorrelation*, $r_{xx}(t)$. The impulse response waveform obtained from the golden circuit (RIR) is sampled and its autocorrelation is computed. The xy-location of the peak value of this autocorrelation function is taken as the defect free reference value. The IR of the DUT is cross-correlated with the RIR and the peak xy-location of the resulting waveform is compared to the one obtained using the autocorrelation of the RIR. Statistically derived thresholds are then used for differentiating between defect-free and defective devices based on these peak xy-locations.

3.1 Differentiation Circuit

In this section we discuss the DFT structure which mainly consists of the differentiation circuit implemented using a single operational amplifier (opamp). Figure 4 shows the schematic of the differentiation circuit. The

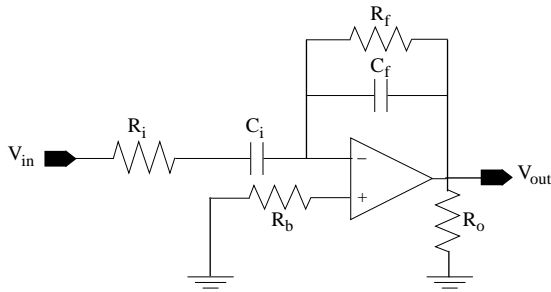


Fig. 4. Differentiator circuit implemented using operational amplifier.

closed loop gain of an ideal differentiator, given by Equation 6, indicates a steady increase of 20dB/decade. The

$$A = -\frac{R_f}{X_i} = -sC_i R_f = -j\omega C_i R_f \quad \text{Eq. 6.}$$

decrease in the input impedance (X_i) with increasing frequency can cause significant increase in the gain. This can cause 1) the circuit to become unstable or 2) amplify the high frequency noise in the input signal causing loss of information at the output. This can be circumvented though the use of C_f and R_i which limit the high frequency gain of the amplifier. The frequency at which the gain of the differentiation circuit is 0dB, f_{0dB} , is given by Equation 7. The

$$f_{0dB} = \frac{1}{2\pi R_f C_i} \quad \text{Eq. 7.}$$

gain limiting frequency, f_{gl} , and the unity gain bandwidth, f_{ug} , of the opamp are given by Equation 8 and 9 respectively. The Figure 5 shows the frequency response of the differentiator circuit on a log scale. The values of R_i , C_i , R_f and C_f are chosen such that $f_{0dB} < f_{gl} < f_{ug}$. The designer

$$f_{gl} = \frac{1}{2\pi R_i C_f} \quad \text{Eq. 8.}$$

$$f_{ug} = \frac{1}{2\pi R_f C_f} \quad \text{Eq. 9.}$$

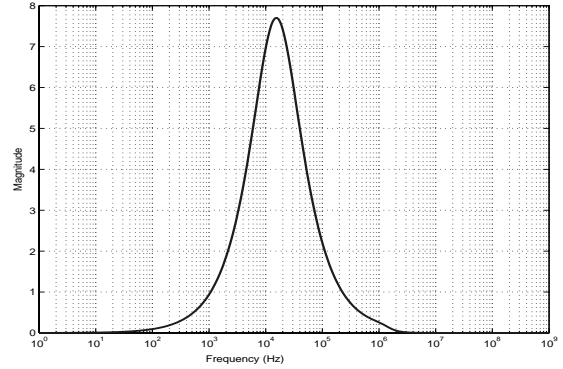


Fig. 5. Frequency response of the opamp differentiator circuit.

must pay attention to select the component values such that the high frequency noise is attenuated to maximum possible extent. Also, the gain of the amplifier must be limited so as to prevent the circuit from saturating which results in non-linear operation.

The impulse response waveform obtained from the differentiation circuit is virtually identical to the ideal impulse response waveform obtained using a DSP based discrete differentiation operation on the sampled IR. Figure 6 shows the output of the differentiation circuit, marked as “*measured IR*”, superimposed on the ideal impulse response, marked as “*ideal IR*”. The finite gain of the differentiation

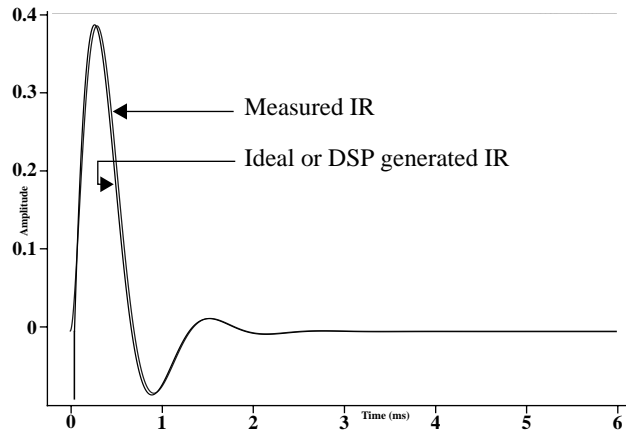


Fig. 6. IR comparison: Ideal using DSP vs. measured using differentiator circuit.

circuit may cause the measured impulse response to appear different from the ideal IR. This is true because, 1) due to

the inverting nature of the differentiation circuit, the measured impulse response gets phase shifted by 180° from the ideal IR and 2) the finite gain of the differentiation circuit limits the amplitude of the output causing the measured impulse response to appear much smaller than the ideal IR. In order to compare the shapes of the two waveforms shown in Figure 6, we inverted and scaled the ideal IR.

4.0 Experimental Design

The test methodology is demonstrated on a benchmark circuit for universal or continuous-time state variable filter obtained from [6]. Figure 7 shows the schematic of the active filter implemented using three opamps. It incorpo-

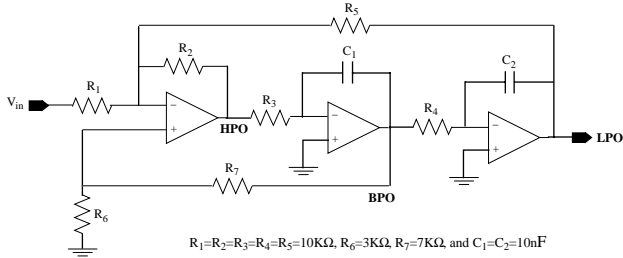


Fig. 7. Circuit diagram of continuous-time state variable active filter or universal filter.

rates high-pass, band-pass and low-pass filters whose outputs are denoted by HPO, BPO and LPO respectively. The values of the components obtained from the benchmark circuit specifications are shown in the figure. The transfer functions of the high-pass, band-pass and low-pass filters are given in Equation 10, 11 and 12 respectively. The fre-

$$H_{LPO}(s) = \frac{K}{s^2 + \frac{1}{QR_3C_1}s + \frac{1}{R_3R_4C_1C_2}} \quad \text{Eq.10.}$$

$$H_{BPO}(s) = \frac{K}{s^2 + \frac{1}{QR_3C_1}s + \frac{1}{R_3R_4C_1C_2}} \quad \text{Eq.11.}$$

$$H_{LPO}(s) = \frac{Ks^2}{s^2 + \frac{1}{QR_3C_1}s + \frac{1}{R_3R_4C_1C_2}} \quad \text{Eq.12.}$$

where

$$K = \frac{2R_6R_7}{R_1R_7 + R_1R_6 + R_6R_7}$$

$$Q = \frac{2R_1R_6}{R_1R_7 + R_1R_6 + R_6R_7}$$

quency response of these filters are shown in Figure 8.

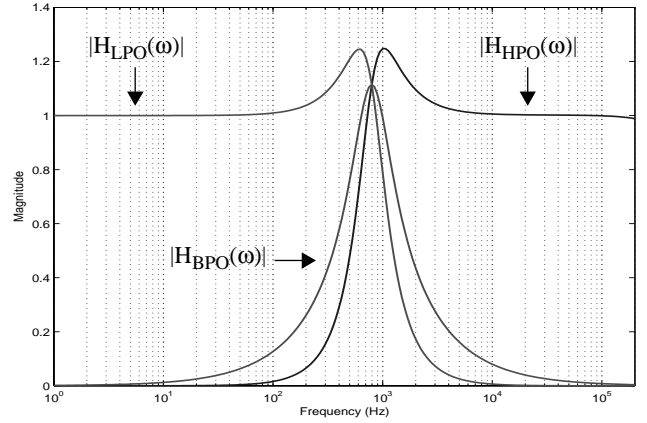


Fig. 8. Frequency response of high-pass, band-pass and low-pass filters as part of the state variable filter.

Without loss of generality, we use this circuit as a low pass filter. Therefore, the defect detection procedure is applied on the signals measured at LPO. This is a conservative approach, as consideration of HPO and BPO can potentially increase the defect detection sensitivity due to increased observability.

5.0 Fault Model And Simulation Setup

A resistive fault model is used to represent open and shorting types of defects. A resistive open fault implies an increase in the resistance between two nodes that are normally shorted with a very low resistive connection. A resistive shorting fault represents an extra resistive connection between any given node in the DUT to either of the supply ($+/-V_{CC}$) nodes or the ground (GND) node. To reduce the number of variables used to generate the defect simulation models, only resistive shorts to ground are considered. The two types of fault models are illustrated in Figure 9 where

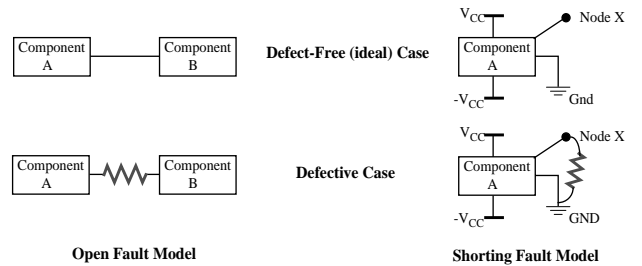


Fig. 9. Resistive Fault Models (a) Resistive Open (b) Resistive Short to GND.

Node X represents any node in the defect-free circuit that is not already shorted to ($+/-$) V_{CC} or GND.

The simulation space consists of three main variables, namely the fault-location, the fault-value and the process model. Ten random defect locations were chosen in the DUT, eight of them were resistive opens and two were resistive shorts. The resistance value of each fault (open and short) was varied to closely represent the severity of the

physical defects and are shown in Table 1. Multiple resistance values of each defect were chosen to evaluate the defect detection sensitivity of our screening mechanism on the defect severity. Thus, totally 50 defects were derived, 40 (8*5) of which were opens and the remaining 10 (2*5) were shorts.

The golden device is basically the defect-free circuit with *typical* circuit and device (resistor and capacitor) parameters. Due to the variability in the fabrication process we expect that both the above mentioned parameters will deviate from their typical values. In order to account for these process variations, 50 defect-free models were generated using Monte Carlo analysis with +/-5% variations in both circuit and device parameters. The devices that have process variations in this *nominal* range form the defect-free population. The device parameters were varied globally, therefore, they do not include simulations for device mismatch. Defect-free devices that have either process variations that exceed this nominal limit, devices that have open or shorting defect with variations within the nominal process limit or have open or shorting defects with excessive process variations are deemed as defective devices.

Table 2 shows number of models, type of defect inserted and percentage process and parameter variations for all these type of defects. Defect model DM1 consists of 4 different types of extreme process (device and circuit parameter) variations without any defects. Model DM2 consists of 21 nominal process (device and circuit parameter) variations with instances of each defect in Table 1 at all possible locations. In other words, each of the 50 defects was simulated in 21 different process models. Out of these, one process model was the golden device model, while the remaining 20 were obtained by varying the process parameters of the golden device within a range of +/-5%. The last defect model, DM3, simulated the 50 defects in 4 extreme process models in which the parameters were varied by +/-25% of the nominal values. Totally 1304 transient simulations were performed on the DUT using the above models.

Opens (Ω)	Shorts (Ω)
10K	1
100K	5
1M	50
10M	100
100M	1K

Table 1: Resistance values for shorting and open defects.

In order to evaluate the defect detection sensitivity of the proposed technique, we compare the number of detections with that of a typical specification based test. For linear analog components, one of the most commonly used performance specification is the variation in their spectral bandwidth. To obtain the bandwidth, we performed ac simulations (frequency sweep) on all the 1304 simulation models described above.

6.0 Experimental Results

A statistical approach based on linear regression analysis is used to derive defect-free thresholds and outlier analysis is used for defect screening. Figure 10 shows a scatter plot of xy-coordinates corresponding to the peak locations of each auto or cross-correlation waveforms obtained from all the defect-free simulations denoted as DF above. The x and y coordinates of each peak location are plotted along x and y axes respectively. The values of x -coordinates corresponding to each point are sorted in ascending order. The regression line is derived as a least-squares fit of a straight line to the defect-free points and is labeled in figure 10. The two curves labeled “prediction limits” in the above figure, represent the 3σ prediction limits defined around the regression line as given by Equation 13. The prediction limits are sensitive to both the number of samples and the amount of dispersion of data points around the regression line (Mean Square Error or MSE). The region enclosed by

Model Type	Process/parameter variations (# of models)	Type of variation	Type/Number of defects	Total # of models
Defect Free (DF)	+/-5% (50)	Monte Carlo	none	50
Defect Model 1 (DM1)	+/- 25% (2) +/-50% (2)	Manually generated	none	4
Defect Model 2 (DM2)	+/-5% (21)	Monte Carlo	5 opens (5 Res. values) 5 shorts (5 Res. values)	1050
Defect Model 3 (DM3)	+/-25% (2) +/-50% (2)	Manually generated	5 opens (5 Res. values) 5 shorts (5 Res. values)	200

Table 2: Defect free and defective device simulation models

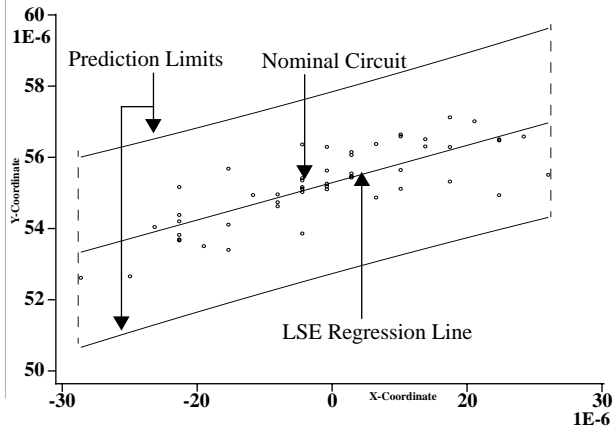


Fig. 10. Scatter plot of xy-coordinates of the peak auto/cross-correlation waveforms obtained from DF simulation model.

$$y = b_0 + b_1 x \pm W \sqrt{MSE} \sqrt{1 + \frac{1}{n} + \frac{(x - \bar{x})^2}{\sum_i (x_i - \bar{x})^2}} \quad \text{Eq.13.}$$

where

$$W = \sqrt{2F((1 - \alpha); 2; (n - 2))}$$

$$\sqrt{MSE} = \sqrt{\frac{\sum_{i=1}^n (Y_i - \hat{Y}_i)^2}{n - 2}} \quad (\text{Mean Square Error})$$

the two prediction limits accounts for the process variations in device and circuit parameters and is used to identify the defect-free devices. It must be realized that the regression analysis shown above establishes *vertical* bounds only on the peak y-values. The bounds along the horizontal direction are derived using the x-values of the data points that are furthest from the nominal (labeled in the figure) on both sides. These limits are shown using two dotted lines on the left and right edge of the scatter plot. If a data point falls inside this four-sided region, the corresponding device is considered defect-free otherwise it is identified as defective.

Based on the discussion of auto/cross-correlation based detection criterion mentioned in section 3.0, it may appear that the autocorrelation of RIR sets up an upper limit on the peak cross-correlation value that can be obtained by cross-correlating the RIR with any other DUT's IR. However, this argument may not hold, particularly when dealing with amplifier circuits. Peak cross-correlation is obtained when the area under the product of the two waveforms is maximum. The peak cross-correlation

value depends on the amplitudes of both the waveforms but the width of only the “narrower” waveform. This suggests that keeping the width of the two waveforms the same while increasing the amplitude of one of the waveforms produces a larger peak (y-value) cross-correlation at the same x-location. In contrast, if the amplitudes are kept same and width of only one of the waveforms is increased, the peak cross-correlation (y-value) remains the same but its x-value increases.

In case of amplifier circuits, varying the device and/or circuit parameters can enhance the amplifier gain resulting in a larger value at the output. This when cross-correlated with the RIR may produce a peak value that is larger than the peak value of the RIR autocorrelation. Figure 11 shows the RIR and IR of a DUT picked from DF model which has been amplified due to the process variations. Also shown in

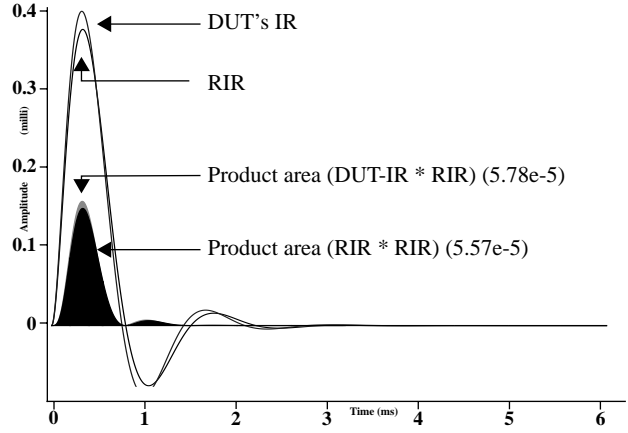


Fig. 11. Effect of process variations in defect-free devices causing increase in the peak cross-correlation value.

the figure are the two product waveforms (filled waveforms) that represent the occurrence of the peak auto/cross-correlation values obtained when the two waveforms overlap in time. One corresponds to the product of RIR with itself and the second corresponds to the product of RIR with the DUT's IR. It is clear that due to the amplification of the DUT's IR, the peak cross-correlation value which corresponds to the area under the product waveform becomes higher than the peak autocorrelation of RIR. In extreme cases, due to the presence of defects and/or excessive process variations, the DUT may amplify the outputs to very high values causing the differentiator circuit to saturate. In such cases, the differentiator circuit no longer behaves as a linear circuit and thus extremely high values of peak cross-correlation may be obtained. Figure 12 shows such an example, where the IR of a DUT with a 10MΩ open-fault, picked from DM3, is shown along with the RIR. The use of regression analysis to establish upper and lower bounds around the defect-free points, naturally eliminates the devices whose peak cross-correlation values are higher

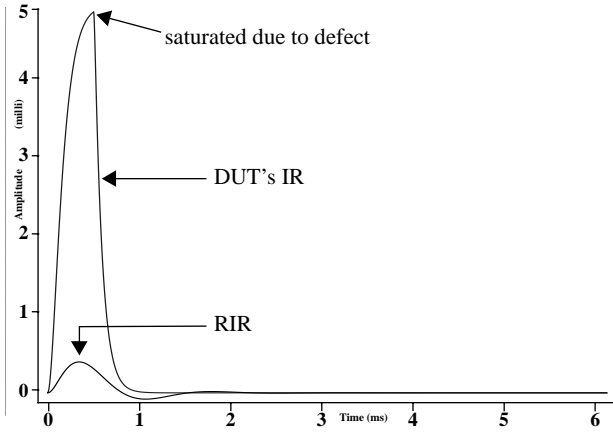


Fig. 12. Effect of process variations and defects causing non-linear behavior.

or lower, by a certain tolerance, than the peak autocorrelation of RIR.

The purpose of the analysis presented in this section is to determine the detection sensitivity of the proposed technique with respect to the severity of the defect reflected by its resistance value. Figure 13 shows the scatter plot of the DF data points along with the data points obtained from DM1, DM2 and DM3. The defect-free points are localized

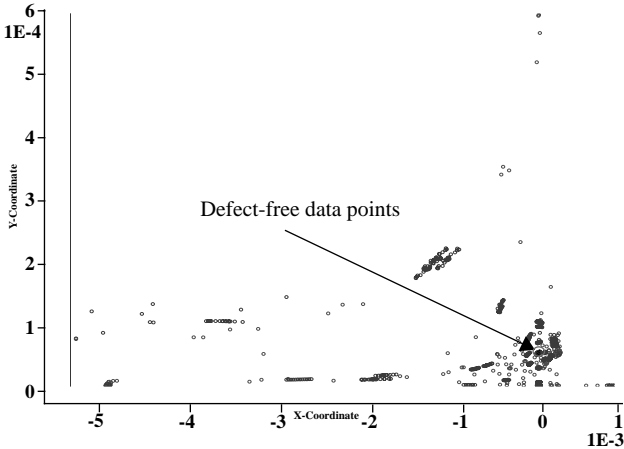


Fig. 13. Scatter plot of xy-coordinates of the peak auto/cross-correlation waveforms obtained from DF, DM1, DM2 and DM3 simulation models.

in a region identified using a circle in the figure. The points that fall outside the circle in the figure correspond to defective devices in DM1, DM2 and DM3. Due to the wide spread of the peak xy-locations, caused by variations in process/circuit parameters and defect values, the defect-free points indicated in the figure are not clearly visible. Figure 14 shows a zoomed-in version of the scatter plot to bring the defect-free point in perspective. It must be noted that the points not shown in this figure are already identified as outliers.

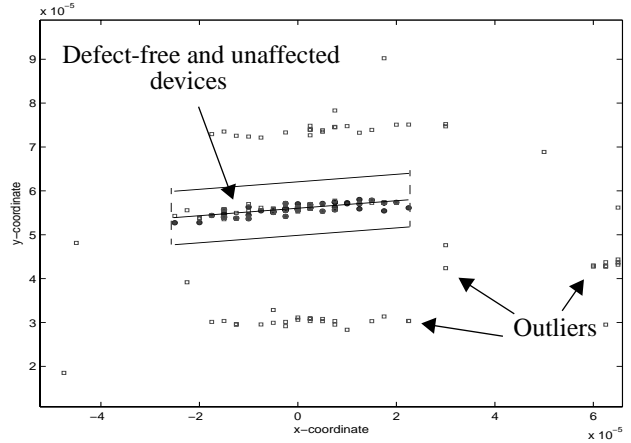


Figure 14. Magnified version of scatter plot shown in Figure 13.

Table 3 shows the number of defects detected in above set of experiments using the proposed outlier analysis. All the defect-free devices in DM1 consisting of excessive process variations are identified as outliers. Similarly, all the devices in DM3 which include defective circuits with excessive process variations are also identified as outliers. However, in case of DM2 which consists of defects with the process variations within the nominal range (+/-5%), some of the imperfections caused by the defect are benign in nature. In such cases the DUT's IR looks similar to RIR. These benign defects include all shorting faults with resistance values of 50, 100 and 1K Ω under all the 21 process models (20 nominal and 1 typical). However, shorting defects with values below 50 Ω , which includes 1 Ω and 5 Ω , and all the open defects with values between 10K to 100M Ω are detected as outliers. For this DUT and set of experi-

Defect Model	# Defective runs	# Defects Detected (Missed)	Type of defects missed	Resistance values of the defect missed
DM1	4	4 (0)	-	-
DM2	1050	924 (126)	Shorting	50, 100, 1K
DM3	200	200 (0)	-	-

Table 3: Number of detections in models DM1, DM2 and DM3 using proposed technique.

ments, it is an interesting result as it suggests that open faults are easier to detect than resistive shorting defects.

It must be realized that reporting the fault-coverage (faults detected/total number of faults) in the above case is not very meaningful because the total number of defects detected can be artificially inflated by increasing the number of defective cases in DM1 or DM3 where all the defects are guaranteed to be detected. However, to make the above results more meaningful we compare the number of defect detected using the proposed technique with a typical specification based or functional test based measurement of the spectral bandwidth of the DUT.

Typical functional specification of most filter circuits allow for a +/-10% of variation in its output bandwidth. However, to be conservative and consistent with our assumed defect-free population in the IR based technique which includes devices with +/-5% (nominal) variations, we calculate the number of functional failures by setting absolute margins of +/-5% around the nominal bandwidth (~1062Hz). All the devices whose bandwidth falls outside the specified range are considered as functional failures. Table 4 lists the number of functional failures detected using the above criteria under each defect simulation model. The specification based test not only misses all the 126 shorting faults that are missed by the proposed technique, but also misses 1) 17 extra shorting defects with values of 1 and 5 Ω (for certain process models and locations) and 2) 24 open defects with all possible values (for certain process models and locations). The above results indicate that the IR based defect detection technique is able to detect all the faults that cause functional violations. In addition it also identifies those faulty devices that are not detected by single parameter (e.g. bandwidth) based specification testing. These defects might be detected by a suite of functional or specification based tests, however our technique provides a means to detect them using a single implicit functional test.

7.0 Conclusions

A simple analog and mixed-signal testing technique based on on-chip generation of impulse response signatures is proposed in this paper. The impulse response is generated by performing on-chip differentiation of the step

response of the circuit. This technique for generating impulse response greatly reduces the cost involved by eliminating the need for complex DFT structures and applying long input patterns. Auto/cross-correlation operations are used to post process the IR signatures obtained from the DUT and a statistical approach is employed for threshold setting and outlier detection. Extensive set of simulations were performed on defect-free and defective circuits that encompassed 1) process variations in DUT's device and circuit parameters, 2) shorting and open defect models, 3) multiple resistance values per defect and 4) multiple defect locations. The defect detection sensitivity of this technique was shown to be better than a classical specification based test performed on the same set of models.

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Defect Model	# Defective runs	# Defects Detected (Missed)	Type of defects missed	Resistance values of the defects missed
DM1	4	4 (0)	-	-
DM2	1050	883 (167)	Shorting Open	1, 5, 50, 100, 1K (shorting) 10K, 100K, 1M, 10M, 100M (open)
DM3	200	198 (2)	Open	100K

Table 4: Number of detections in models DM1, DM2 and DM3 using BW based specification test.