Silicon: Properties and Wafers

Silicon in its pure or *intrinsic* state is a semiconductor, having bulk electrical resistance somewhere between a conductor and an insulator.

Conductivity of silicon can be increased by several orders of magnitude by adding *impurity* atoms into the silicon lattice structure.

- Group III: Boron, use up electrons, referred to as acceptors, leave holes
- Group VI: Arsenic, Phosphorous, provided electrons, referred to as donors

Silicon with majority donors is known as ***n-type*** and that with majority acceptors ***p-type***.

Basic raw material required is a ***wafer*** or disk of silicon, 75 - 300 mm diameter, 1 mm thick.

Wafers are cut from ingots of single-crystal silicon that have been pulled from a crucible melt of pure molten silicon (***Czochralski*** method).

Controlled amounts of impurities are added to the melt to provide the required electrical properties.

A seed crystal is used to create the ingot, growth rate of 30 to 180mm/hour.

Photolithography

Masks are used to define the different regions in the device. Masks are created using data provided by the layout engineer.

Mask are used to isolate regions, the properties of which are either changed or kept the same during various processing steps in contrast to the regions not covered by the mask.

The patterning is achieved by a process called ***photolithography***.

The regions of interest are defined on wafer using a materials called ***photoresist***.

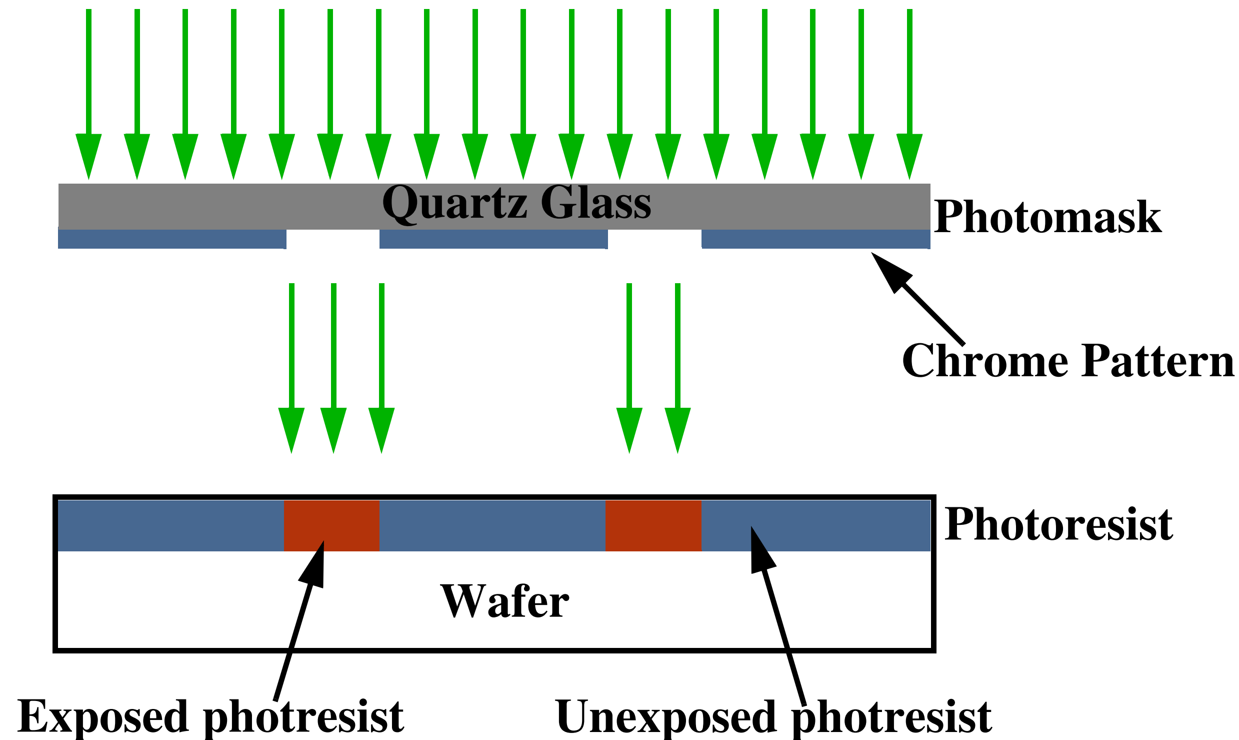
The wafer is coated with the photoresist and subjected to selective illumination through the ***photomask***.

A photomask is constructed with chromium (chrome) covered quartz glass.

A UV light source is used to expose the photoresist. The photomask has chrome where light should be blocked.

The organic photoresist is exposed to the light in regions where the chrome is not present.

Photolithography



A developer solvent is used to dissolve the soluble unexposed photoresist, leaving islands of insoluble exposed photoresist. Called ***negative photoresist***.

A ***positive*** photoresist is initially insoluble, and when exposed to UV becomes soluble.

Photolithography

Photomask is commonly called a ***reticle*** and is usually smaller than the wafer.

A ***stepper*** moves the reticle to successive locations to completely expose the wafer.

Projection printing is normally used, in which lenses between the reticle and wafer focus the pattern on the wafer surface.

Older techniques include ***contact printing*** and ***proximity printing***.

The wavelength of the light source influence the minimum feature size.

- 1980's, mercury lamps with 436 nm or 365nm wavelength.
- 0.25 - 0.18 µm node, excimer lasers with 248 nm (deep ultraviolet).
- Currently, 193 nm argon-fluoride lasers are used for critical layers, e.g. gate poly, source/drain diffusion, first metal.
- 157 nm flouride lasers and 13.4 nm extreme UV (EUV) needed for future processes.

UV steppers and masks are becoming very expensive with each technology generation.

Photolithography

Wavelengths comparable to or greater than the feature size cause distortion in the patterns exposed on the photoresist.

Resolution Enhancement techniques precompensate for this distortion. Performed by modifying amplitude, phase, or direction or incoming light.

Cause ends of line to receive less light than the center, causing nonuniform exposure.

Optical Proximity Correction (OPC) makes small changes to the patterns on the masks to compensate for these local distortions.

Phase Shift Masks (PSM) vary the thickness of the mask to change the phase such that light from adjacent lines are out of phase and cancel where no light is desired.

Off-axis illumination can also improve contrast for certain types of dense, repetitive patterns.

Using a combination of these techniques, the resolution can be extended to 1/8th the wavelength of the light !!!

Well and Channel Formation

Varying proportions of donor and acceptor impurities can be achieved using:

- *Epitaxy*: Involves growing a single-crystal film on the silicon surface by subjecting it to elevated temperatures and a source of dopant material.

- *Deposition*: Dopant material placed onto the silicon surface and then driven into the bulk using a thermal diffusion step.

  Chemical Vapor Deposition (CVD) used for deposition. Heated gases react in the activity of the wafer and produce a product that is deposited on the silicon surface.

- *Ion Implantation*: Silicon substrate subjected to highly energized donor or acceptor atoms.

  Atoms impinge silicon surface forming regions with varying concentrations.

  At elevated temperatures (> 800° C), diffusion occurs between silicon regions having different densities of impurities.

  High-temperature annealing step is required to redistribute dopants uniformly.

  Standard method today for well and source/drain formation.

Silicon Dioxide (SiO_2)

SiO_2 extremely important for many structures and manufacturing techniques.

Various thicknesses required, thin oxides for gates, thicker oxides for high voltage devices and even more thicker oxides to ensure that transistors are not formed unintentionally.

Oxidation of silicon is achieved by heating silicon wafers in an oxidizing atmosphere.

Wet Oxidation: oxidizing atmosphere contains water vapor at temperatures between 900 to 1000°C. Very rapid process. Used for thick field oxides.

Dry Oxidation: oxidizing atmosphere is pure oxygen at temperatures of 1200°C. Produces better quality oxide than wet oxidation. Used for thin, highly controlled oxides.

Atomic Layer Deposition (ALD): a process in which a thin chemical layer is attached to a surface and then a chemical is introduced to produce a thin layer of the required layer. Still an emerging R&D process.

Oxidation (except ALD) consumes silicon and grows almost equally in both vertical directions. Thus oxide projects above and below the original unoxidized silicon surface.

Isolation

Individual CMOS devices need to be isolated to avoid unexpected interactions.

Thick field oxide, is used to raise the threshold voltage above the supply voltage and so prevents a channel from forming.

Additionally, the substrate in the areas where transistors are not required is implanted with impurity concentration to create a ***channel-stop*** diffusion.

LOCOS or Local Oxidation of Silicon was used to produce varying oxide thickness in older technologies

Processes below, 180 nm achieve isolation by forming insulating trenches of SiO_2 that surround active areas. Referred as ***Shallow Trench Isolation (STI)***.

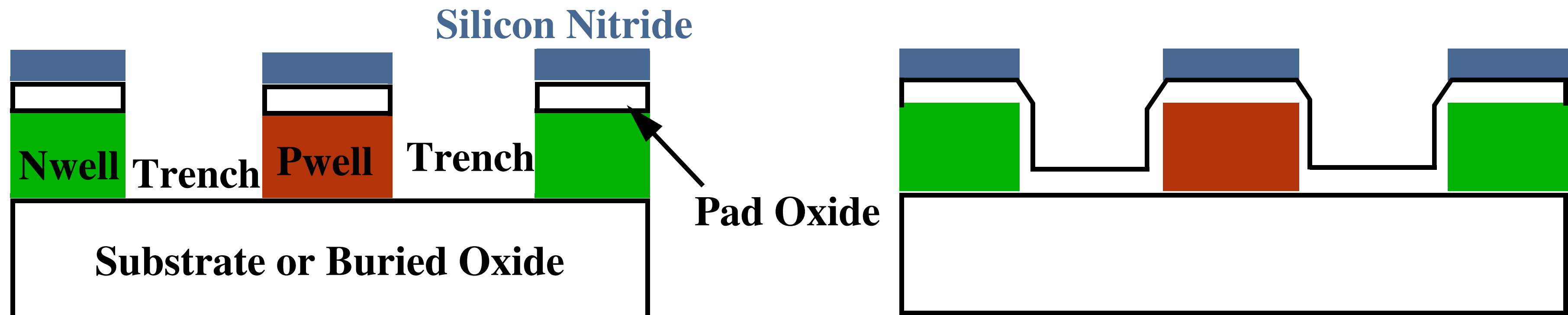
STI starts with a pad oxide and a silicon nitride layer, which act as the masking layers.

Opening in pad oxide are used to do the etching. A linear oxide layer is then grown.

Trenches are filled with SiO_2 using CVD (does not consume silicon).

Isolation

Pad oxide and the nitride layers are removed and *Chemical Mechanical Polishing (CMP)* is used to planarize the structure.

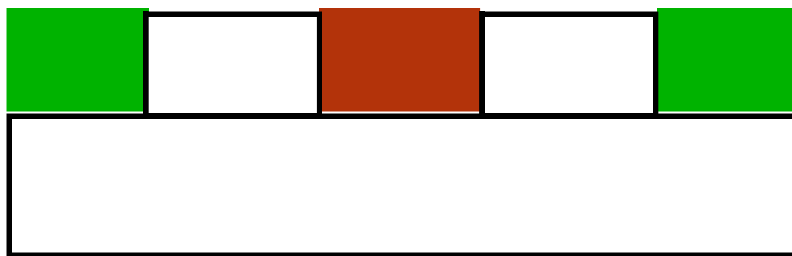


(A) Trench Etch

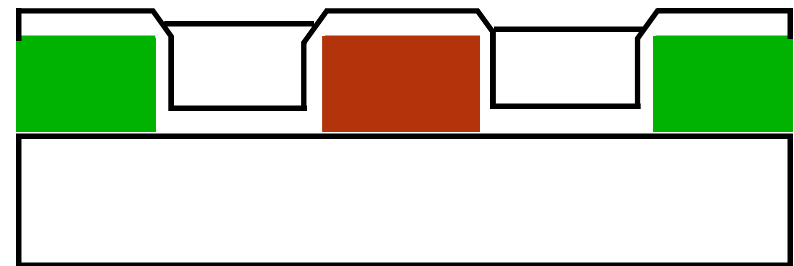
(B) Linear Oxidation

Shallow Trench Isolation (STI)

(D) CMP for planarization

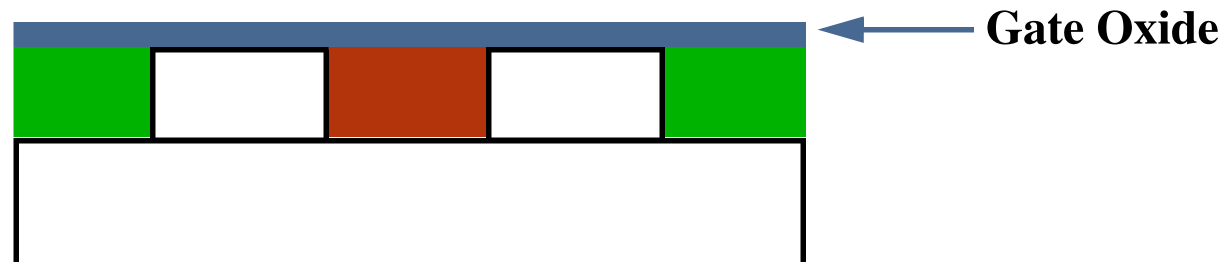


(C) Trenches Filled with CVD



Gate Oxide

For STI-defined source/drain regions, the gate oxide is grown on top of the planarized structure. This oxide structure is called the ***gate stack***.



Called gate stack, as pure SiO_2 gate oxide is not used.

- Rather, a stack is formed containing a few atomic layers of SiO_2 overlaid with few layers of oxynitrided oxide (has nitrogen added).
- Presence of nitrogen increases the dielectric constant, thus decreasing the effective oxide thickness (EOT).

Modern processes provide at least two oxide thicknesses

- Thin for logic, thick for I/O
- Some might provide two thicknesses for logic (speed vs leakage tradeoff).

At 65 nm node, effective thickness of thin gate oxide is of the order of 1.5 nm !!!

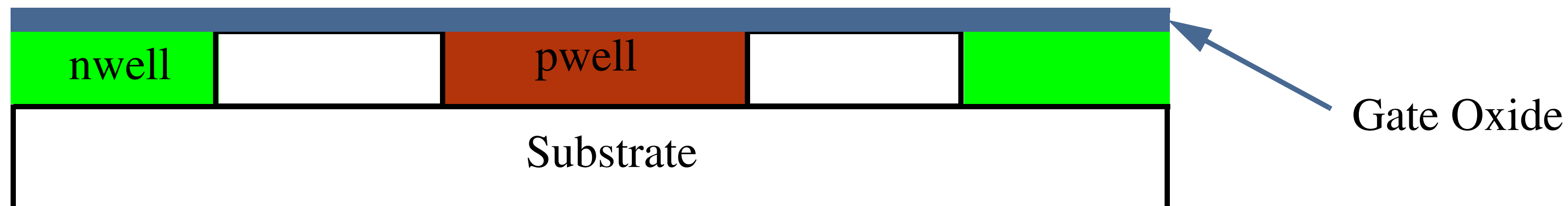
Gate and Source/Drain Formation

Today gate material is ***polysilicon*** or simply ***poly***

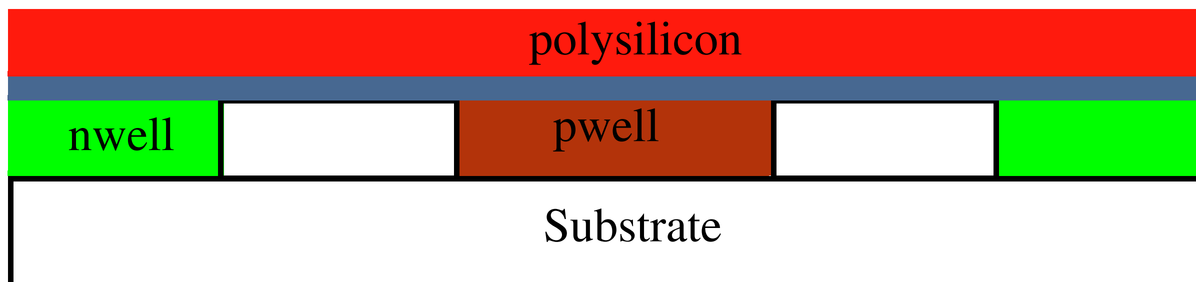
- Formed by depositing silicon on SiO_2 or other surfaces without crystal orientation.
- Annealing process used to control size of the single crystal domain and quality
- High resistance, therefore is doped with impurities or combined with refractory metal

Polysilicon gate serves as a mask to allow precise alignment of the source and drain
Called ***self-aligned polysilicon gate*** process.

Gate oxide grown where transistors are required

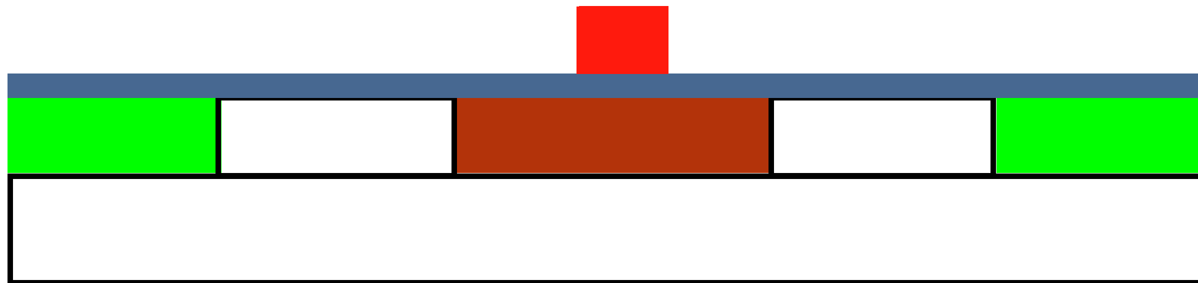


Deposit polysilicon

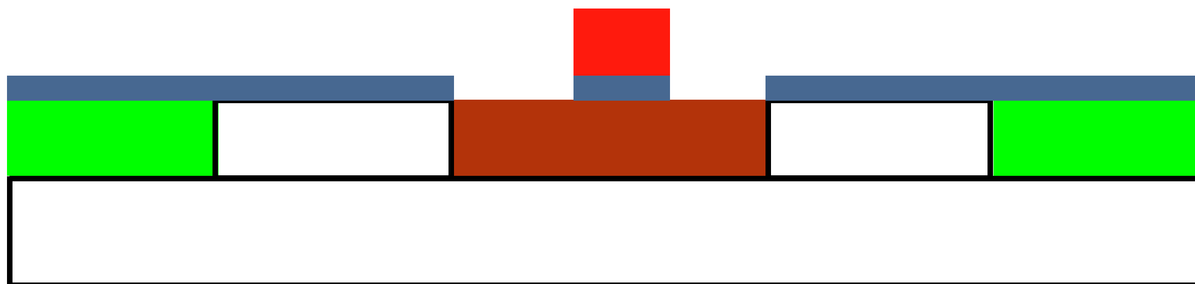


Gate and Source/Drain Formation

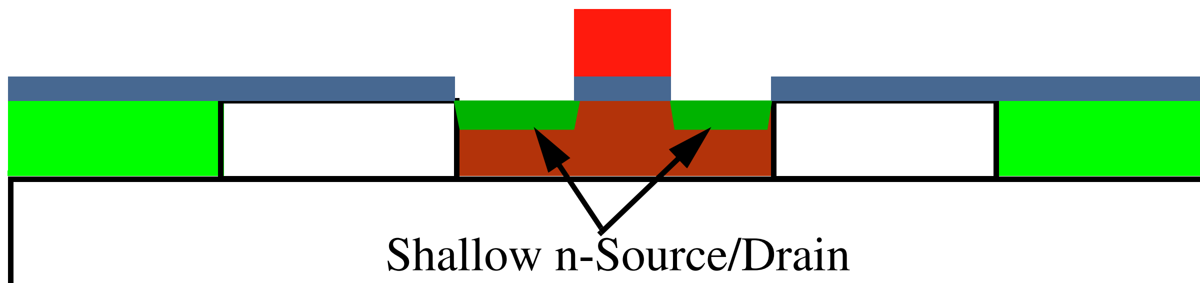
Pattern Polysilicon



Etch Exposed gate oxide



Implant source/drain regions

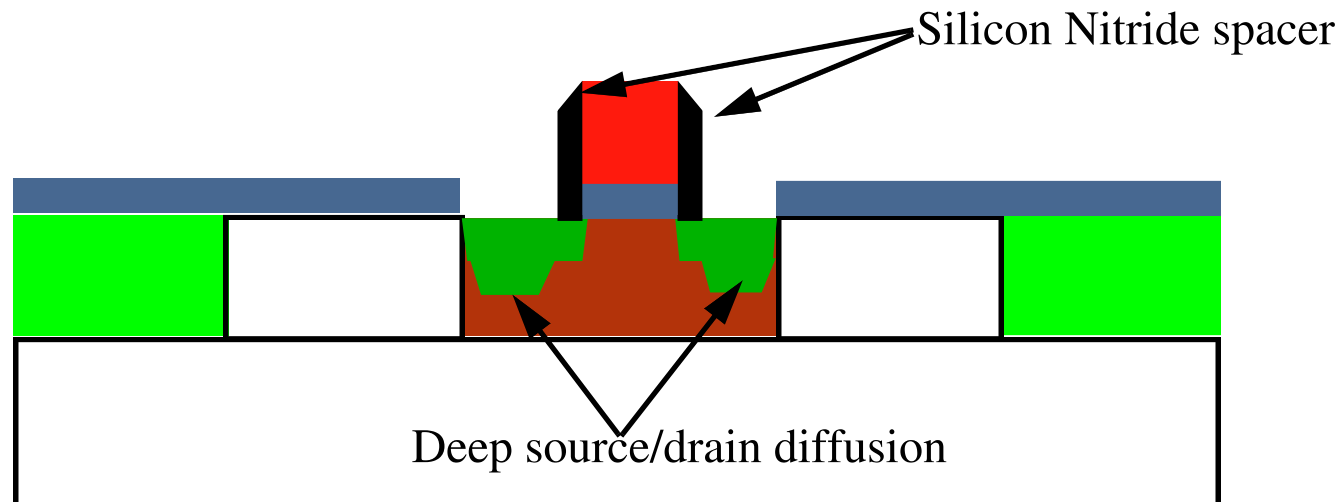


Gate and Source/Drain Formation

The source/drain implant is relatively low, called ***lightly doped drain (LDD)*** structure.

- Reduces electric field at drain junction improving immunity to hot electrons
- Low capacitance but high resistance, reduces device performance
- More heavily doped source/drain required to provide devices with good performance and immunity to hot electrons

A silicon nitride (Si_3N_4) ***spacer*** along the edge of gate serves as mask for deeper diffusion



Gate and Source/Drain Formation

Gate and source/drain diffusion regions have high resistance. A surface of a ***refractory metal*** on silicon can reduce resistance

Refractory metal has high melting point e.g. tantalum, molybdenum, titanium or cobalt.

Silicide layer is formed when the two substances react at elevated temperature.

Process is called ***salicide (self-aligned silicide)*** and both gate and drain/source are silicided.

In ***polycide*** process, only the gate is silicided.

Normally poly over diffusion forms a transistor, so a short metal1 wire is necessary to connect diffusion output node to a poly input node.

Some processes allow a contact region between the silicided gate and source/drain.

Known as ***local interconnect*** and very useful for dense cell layouts, especially SRAMs.

Contacts, Metallization and Passivation

Contact cuts are made to source, drain and gate and filled with tungsten. Wires in older technologies were Aluminum.

Metallization involves building wires.

Al deposited either by ***evaporating*** or ***sputtering***.

- Evaporation is performed by high electrical current in a thick Al wire in vacuum chamber. Some Al atoms are vaporized and deposited on the wafer. A better technique is to use a focused electron beam to evaporate Al.
- Sputtering is achieved by generating a gas plasma by ionizing an inert gas using an RF or DC electric field. The ions are focussed on Al target and the plasma dislodges metal atoms.

Wet or dry etching is used to remove unwanted metal.

Finally, a protective glass layer called the ***passivation*** or ***overglass*** is added at the top.

Opening in the passivation layer allow connections to the I/O pads and test probe points.