Digital Logic II:
Semiconductors, Transistors, Gates, and Adders

CMSC 313
Sections 01, 02

Semiconductors, Transistors, and Gates

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Semiconductors, Transistors, and Gates

- How do we make gates???

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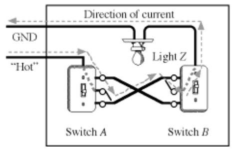
Truth Tables

- Developed in 1854 by George Boole
- further developed by Claude Shannon (Bell Labs)
- Outputs are computed for all possible input combinations (how many input combinations are there?

Consider a room with two light switches. How must they work†?



Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

†Don't show this to your electrician, or wire your house this way. This circuit definitely violates the electric code. The practical circuit never leaves the lines to the light "hot" when the light is turned off. Can you figure how?

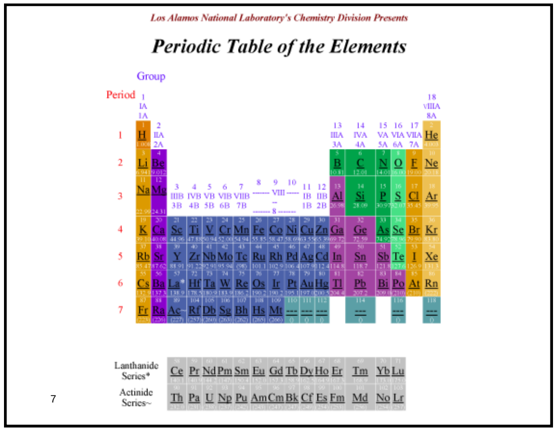
Electrically Operated Switch

- **Example: a relay**

source: http://www.howstuffworks.com/relay.htm

Semiconductors

- **Electrical properties of silicon**
- **Doping: adding impurities to silicon**
- **Diodes and the P-N junction**
- **Field-effect transistors**


Los Alamos National Laboratory's Chemistry Division Presents
Periodic Table of the Elements
Group
Period
Lanthanide Series*
Actinide Series~
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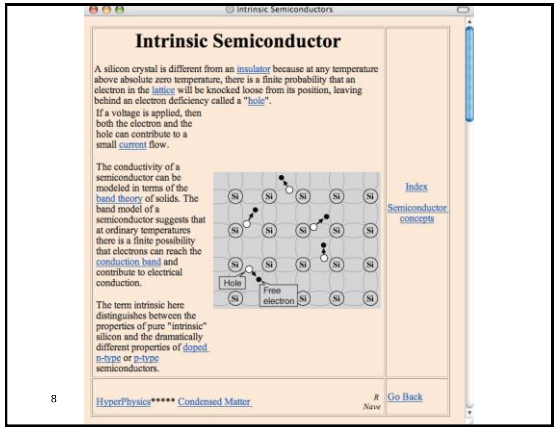
Intrinsic Semiconductors
Intrinsic Semiconductor
A silicon crystal is different from an insulator because at any temperature above absolute zero temperature, there is a finite probability that an electron in the lattice will be knocked loose from its position, leaving behind an electron deficiency called a "hole".
If a voltage is applied, then both the electron and the hole can contribute to a small current flow.
The conductivity of a semiconductor can be modeled in terms of the band theory of solids. The band model of a semiconductor suggests that at ordinary temperatures there is a finite possibility that electrons can reach the conduction band and contribute to electrical conduction.
The term intrinsic here distinguishes between the properties of pure "intrinsic" silicon and the dramatically different properties of doped n-type or p-type semiconductors.
Hole
Free electron
Si
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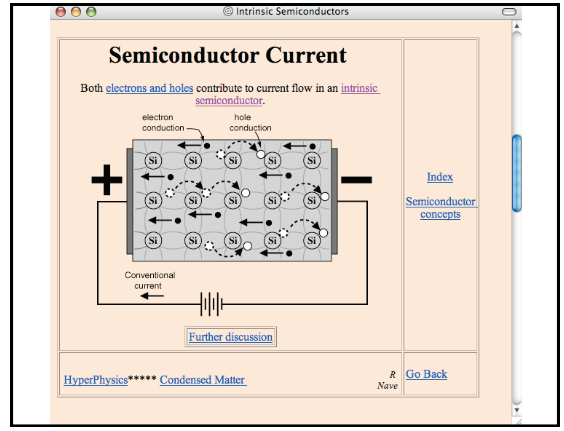
Intrinsic Semiconductors
Semiconductor Current
Both electrons and holes contribute to current flow in an intrinsic semiconductor.
electron conduction
hole conduction
Si
+
−
Conventional current
Further discussion
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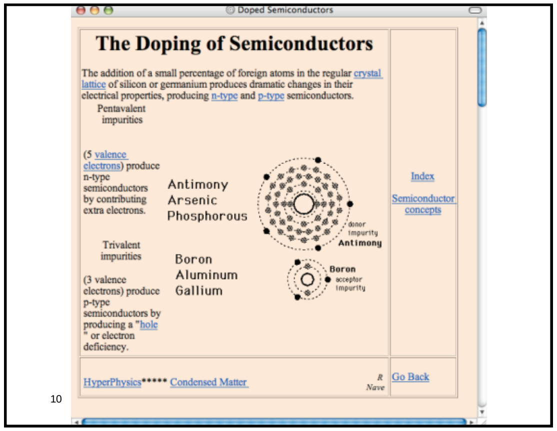
Doped Semiconductors
The Doping of Semiconductors
The addition of a small percentage of foreign atoms in the regular crystal lattice of silicon or germanium produces dramatic changes in their electrical properties, producing n-type and p-type semiconductors.
Pentavalent impurities
(5 valence electrons) produce n-type semiconductors by contributing extra electrons.
Antimony
Arsenic
Phosphorous
donor impurity
Antimony
Trivalent impurities
(3 valence electrons) produce p-type semiconductors by producing a "hole" or electron deficiency.
Boron
Aluminum
Gallium
Boron
acceptor impurity
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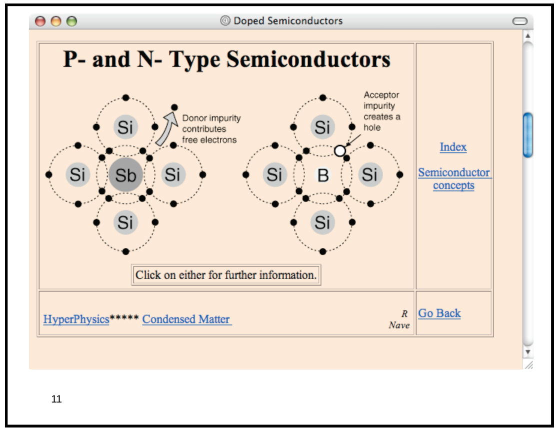
Doped Semiconductors
P- and N- Type Semiconductors
Si
Si
Sb
Si
Si
Donor impurity contributes free electrons
Acceptor impurity creates a hole
Si
Si
B
Si
Si
Click on either for further information.
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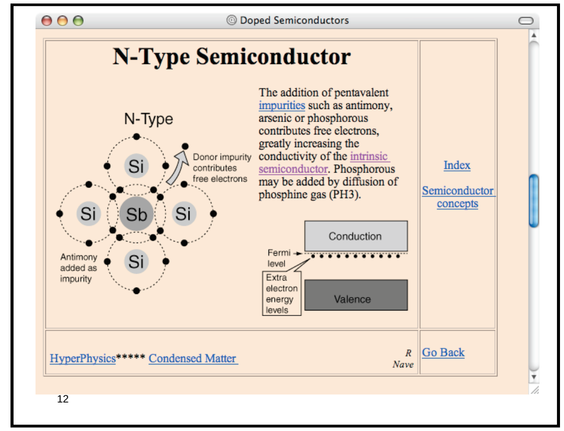
Doped Semiconductors
N-Type Semiconductor
N-Type
Si
Si
Sb
Si
Si
Donor impurity contributes free electrons
Antimony added as impurity
The addition of pentavalent impurities such as antimony, arsenic or phosphorous contributes free electrons, greatly increasing the conductivity of the intrinsic semiconductor. Phosphorous may be added by diffusion of phosphine gas (PH3).
Conduction
Fermi level
Extra electron energy levels
Valence
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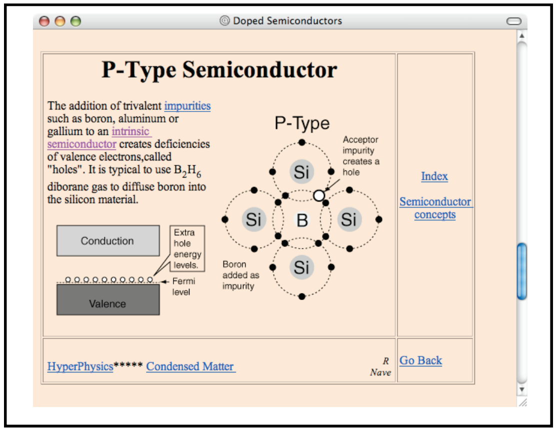

Doped Semiconductors
P-Type Semiconductor
The addition of trivalent impurities such as boron, aluminum or gallium to an intrinsic semiconductor creates deficiencies of valence electrons,called "holes". It is typical to use B_2H_6 diborane gas to diffuse boron into the silicon material.
P-Type
Acceptor impurity creates a hole
Si
B
Conduction
Extra hole energy levels.
Fermi level
Valence
Boron added as impurity
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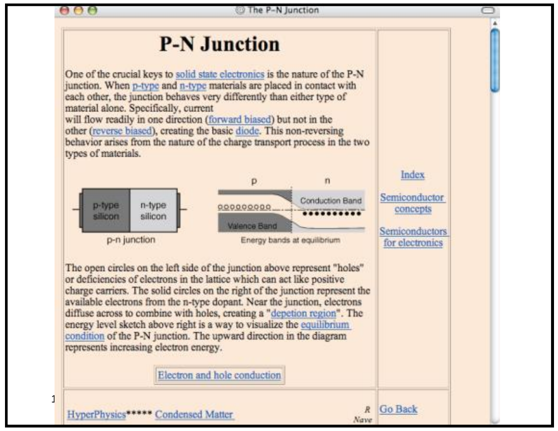

The P-N Junction
P-N Junction
One of the crucial keys to solid state electronics is the nature of the P-N junction. When p-type and n-type materials are placed in contact with each other, the junction behaves very differently than either type of material alone. Specifically, current will flow readily in one direction (forward biased) but not in the other (reverse biased), creating the basic diode. This non-reversing behavior arises from the nature of the charge transport process in the two types of materials.
p-type silicon
n-type silicon
p-n junction
p
n
Conduction Band
Valence Band
Energy bands at equilibrium
The open circles on the left side of the junction above represent "holes" or deficiencies of electrons in the lattice which can act like positive charge carriers. The solid circles on the right of the junction represent the available electrons from the n-type dopant. Near the junction, electrons diffuse across to combine with holes, creating a "depetion region". The energy level sketch above right is a way to visualize the equilibrium condition of the P-N junction. The upward direction in the diagram represents increasing electron energy.
Electron and hole conduction
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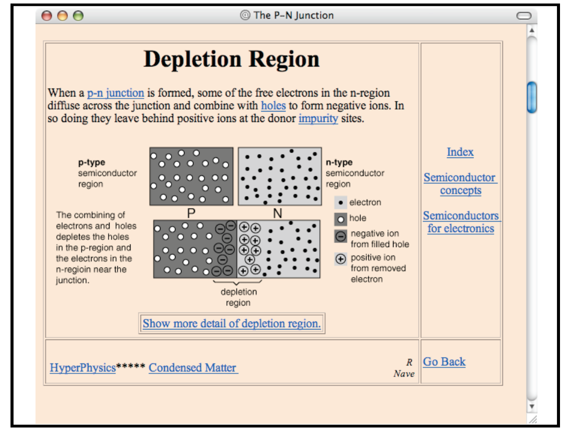

The P-N Junction
Depletion Region
When a p-n junction is formed, some of the free electrons in the n-region diffuse across the junction and combine with holes to form negative ions. In so doing they leave behind positive ions at the donor impurity sites.
p-type semiconductor region
n-type semiconductor region
P
N
The combining of electrons and holes depletes the holes in the p-region and the electrons in the n-regioin near the junction.
electron
hole
negative ion from filled hole
positive ion from removed electron
depletion region
Show more detail of depletion region.
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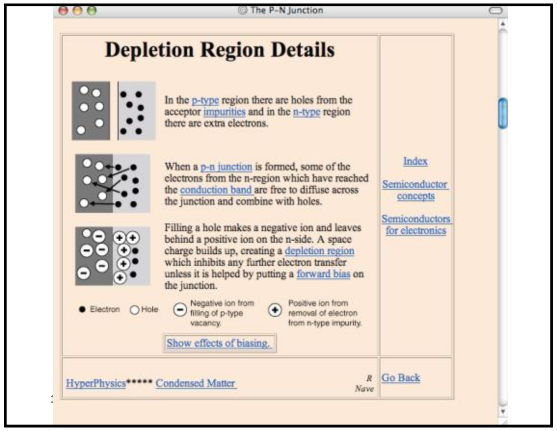
The P-N Junction
Depletion Region Details
In the p-type region there are holes from the acceptor impurities and in the n-type region there are extra electrons.
When a p-n junction is formed, some of the electrons from the n-region which have reached the conduction band are free to diffuse across the junction and combine with holes.
Filling a hole makes a negative ion and leaves behind a positive ion on the n-side. A space charge builds up, creating a depletion region which inhibits any further electron transfer unless it is helped by putting a forward bias on the junction.
Electron
Hole
Negative ion from filling of p-type vacancy.
Positive ion from removal of electron from n-type impurity.
Show effects of biasing.
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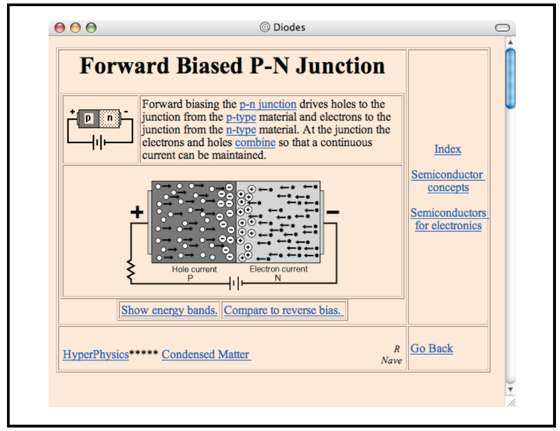
Diodes
Forward Biased P-N Junction
Forward biasing the p-n junction drives holes to the junction from the p-type material and electrons to the junction from the n-type material. At the junction the electrons and holes combine so that a continuous current can be maintained.
p
n
Hole current
P
Electron current
N
Show energy bands.
Compare to reverse bias.
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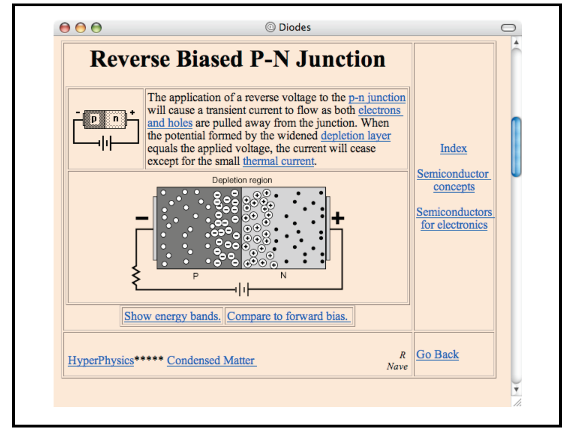
Diodes
Reverse Biased P-N Junction
The application of a reverse voltage to the p-n junction will cause a transient current to flow as both electrons and holes are pulled away from the junction. When the potential formed by the widened depletion layer equals the applied voltage, the current will cease except for the small thermal current.
p
n
Depletion region
P
N
Show energy bands.
Compare to forward bias.
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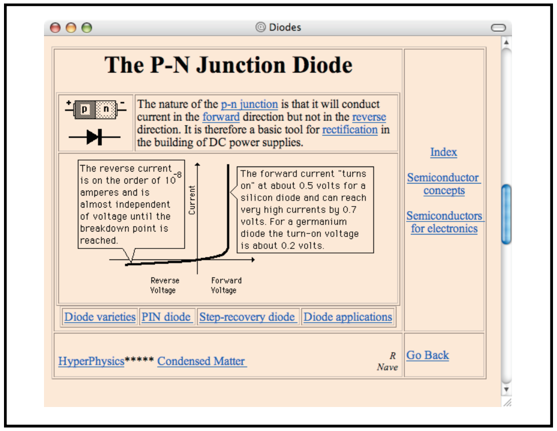
Diodes
The P-N Junction Diode
The nature of the p-n junction is that it will conduct current in the forward direction but not in the reverse direction. It is therefore a basic tool for rectification in the building of DC power supplies.
The reverse current is on the order of 10^-8 amperes and is almost independent of voltage until the breakdown point is reached.
The forward current "turns on" at about 0.5 volts for a silicon diode and can reach very high currents by 0.7 volts. For a germanium diode the turn-on voltage is about 0.2 volts.
Current
Reverse Voltage
Forward Voltage
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PIN diode
Step-recovery diode
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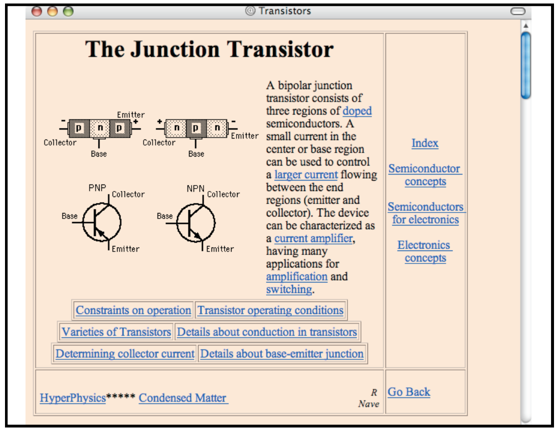
Transistors
The Junction Transistor
A bipolar junction transistor consists of three regions of doped semiconductors. A small current in the center or base region can be used to control a larger current flowing between the end regions (emitter and collector). The device can be characterized as a current amplifier, having many applications for amplification and switching.
Emitter
Collector
Base
PNP
NPN
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Transistor operating conditions
Varieties of Transistors
Details about conduction in transistors
Determining collector current
Details about base-emitter junction
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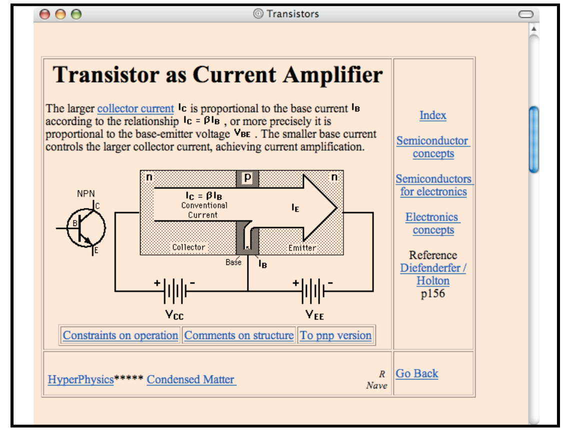
Transistors
Transistor as Current Amplifier
The larger collector current I_C is proportional to the base current I_B according to the relationship $I_C = \beta I_B$, or more precisely it is proportional to the base-emitter voltage V_{BE}. The smaller base current controls the larger collector current, achieving current amplification.
NPN
$I_C = \beta I_B$
Conventional Current
I_E
I_B
Collector
Base
Emitter
V_{CC}
V_{EE}
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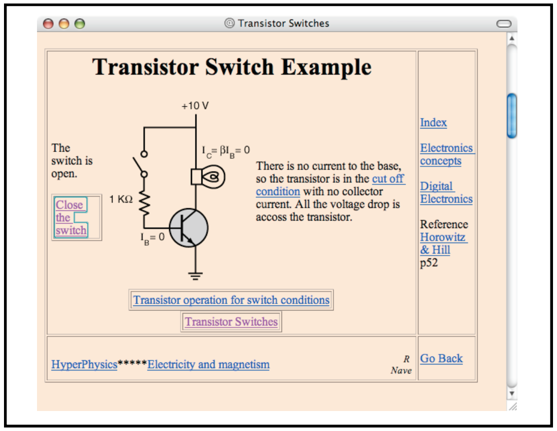
Transistor Switches
Transistor Switch Example
+10 V
The switch is open.
$I_C = \beta I_B = 0$
There is no current to the base, so the transistor is in the cut off condition with no collector current. All the voltage drop is across the transistor.
Close the switch
1 KΩ
$I_B = 0$
Transistor operation for switch conditions
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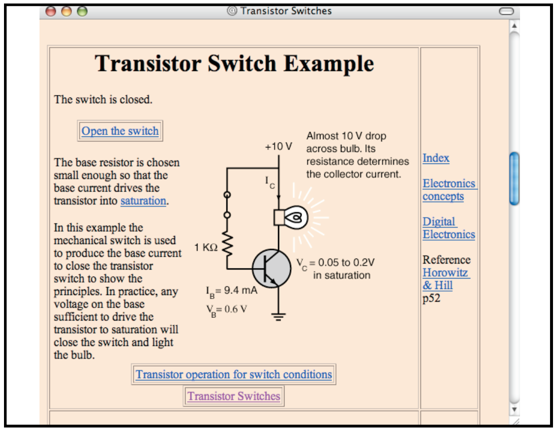
Transistor Switches
Transistor Switch Example
The switch is closed.
Open the switch
The base resistor is chosen small enough so that the base current drives the transistor into saturation.
In this example the mechanical switch is used to produce the base current to close the transistor switch to show the principles. In practice, any voltage on the base sufficient to drive the transistor to saturation will close the switch and light the bulb.
+10 V
Almost 10 V drop across bulb. Its resistance determines the collector current.
I_C
1 KΩ
V_C = 0.05 to 0.2V in saturation
I_B = 9.4 mA
V_B = 0.6 V
Transistor operation for switch conditions
Transistor Switches
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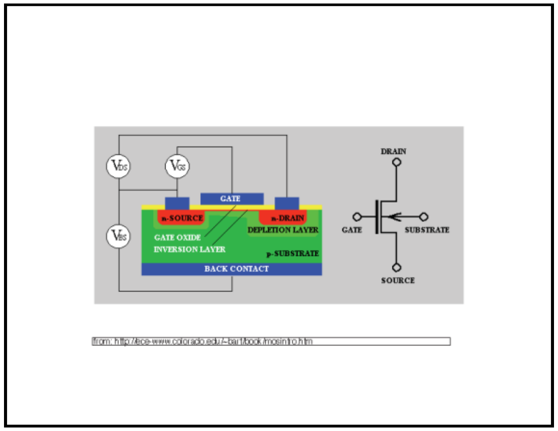
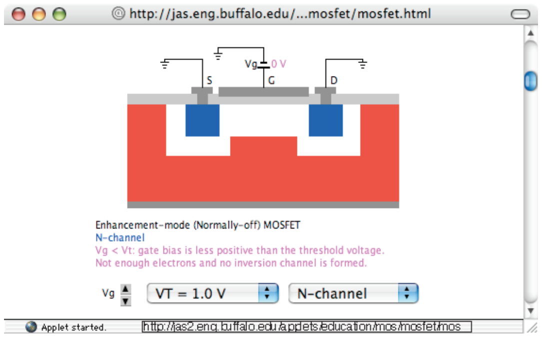

V_{DS}
V_{GS}
V_{BS}
GATE
n-SOURCE
n-DRAIN
DEPLETION LAYER
GATE OXIDE
INVERSION LAYER
p-SUBSTRATE
BACK CONTACT
DRAIN
GATE
SUBSTRATE
SOURCE
from: http://ece-www.colorado.edu/~bart/book/mosintro.htm



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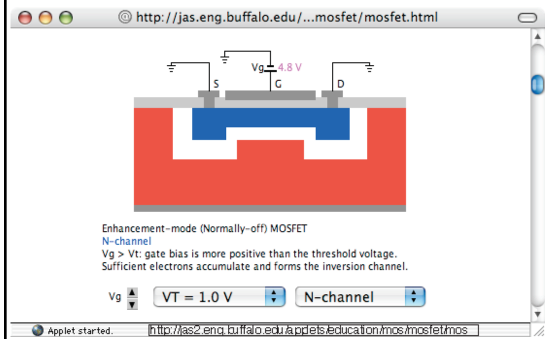

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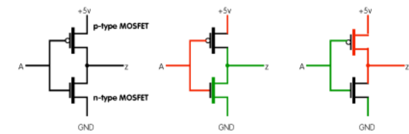
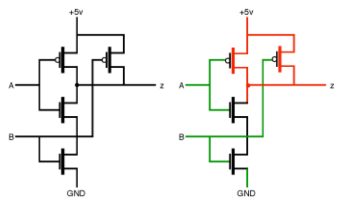
An Inverter using MOSFET

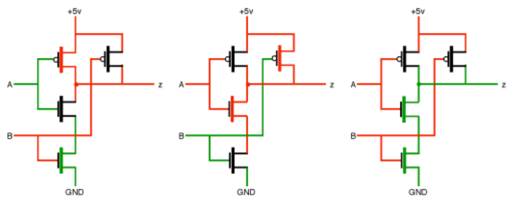
- CMOS = complementary metal oxide semiconductor
- P-type transistor conducts when gate is low
- N-type transistor conducts when gate is high

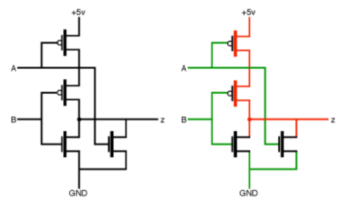




NAND GATE

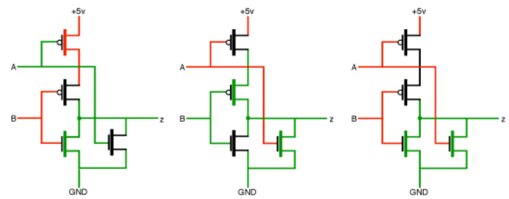
A	B	z
0	0	1
0	1	1
1	0	1
1	1	0





NOR GATE

A	B	z
0	0	1
0	1	0
1	0	0
1	1	0



CMOS Logic vs Bipolar Logic

- MOSFET transistors are easier to miniaturize
- CMOS logic has lower current drain
- CMOS logic is easier to manufacture

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Circuits for Addition

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3.5 Combinational Circuits

- Combinational logic circuits give us many useful devices.
- One of the simplest is the *half adder*, which finds the sum of two bits.
- We can gain some insight as to the construction of a half adder by looking at its truth table, shown at the right.

Inputs		Outputs	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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Half Adder

- Inputs: A and B
- Outputs: S = lower bit of $A+B$, c_{out} = carry bit

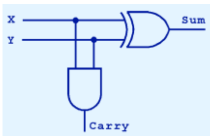
A	B	S	c_{out}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- Using Sum-of-Products: $S = \overline{A}B + A\overline{B}$, $c_{\text{out}} = AB$.
- Alternatively, we could use XOR: $S = A \oplus B$.

1

3.5 Combinational Circuits

- As we see, the sum can be found using the XOR operation and the carry using the AND operation.



Inputs		Outputs	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3.5 Combinational Circuits

- We can change our half adder into to a full adder by including gates for processing the carry bit.
- The truth table for a full adder is shown at the right.

Inputs			Outputs	
X	Y	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder

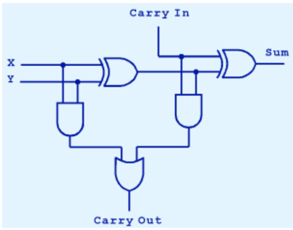
- Inputs: A, B and c_{in}
- Outputs: $S =$ lower bit of $A + B$, $c_{\text{out}} =$ carry bit

A	B	c_{in}	S	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- $S = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + ABC = A \oplus B \oplus C.$
- $c_{\text{out}} = \text{MAJ3} = AB + BC + AC.$

3.5 Combinational Circuits

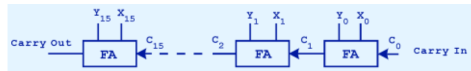
- Here's our completed full adder.



Inputs			Outputs	
X	Y	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3.5 Combinational Circuits

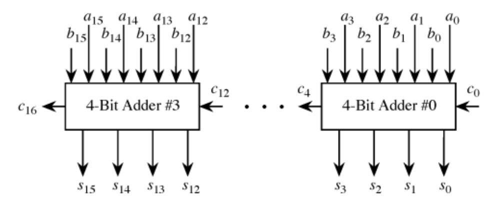
- Just as we combined half adders to make a full adder, full adders can connected in series.
- The carry bit "ripples" from one adder to the next; hence, this configuration is called a *ripple-carry adder*.



Today's systems employ more efficient adders.

Constructing Larger Adders

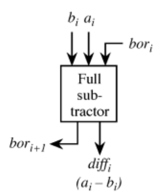
- **A 16-bit adder can be made up of a cascade of four 4-bit ripple-carry adders.**



Full Subtractor

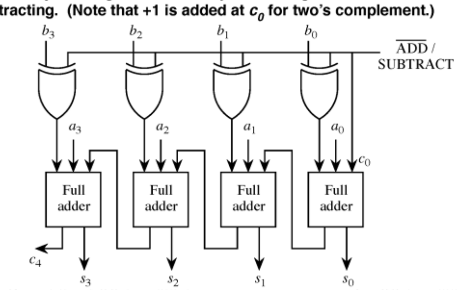
- Truth table and schematic symbol for a ripple-borrow subtractor:

a_i	b_i	bor_i	$diff_i$	bor_{i+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Combined Adder/Subtractor

- A single ripple-carry adder can perform both addition and subtraction, by forming the two's complement negative for *B* when subtracting. (Note that +1 is added at c_0 for two's complement.)



Carry-Lookahead Addition

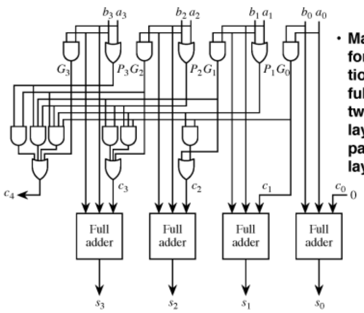
$$s_i = \overline{a_i}\,\overline{b_i}c_i + \overline{a_i}b_i\overline{c_i} + a_i\overline{b_i}\,\overline{c_i} + a_ib_ic_i$$
$$c_{i+1} = b_ic_i + a_ic_i + a_ib_i$$
$$c_{i+1} = a_ib_i + (a_i + b_i)c_i$$
$$c_{i+1} = G_i + P_ic_i$$

- Carries are represented in terms of G_i (generate) and P_i (propagate) expressions.

$$G_i = a_ib_i \quad \text{and} \quad P_i = a_i + b_i$$
$$c_0 = 0$$
$$c_1 = G_0$$
$$c_2 = G_1 + P_1G_0$$
$$c_3 = G_2 + P_2G_1 + P_2P_1G_0$$
$$c_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$

3-22 Chapter 3: Arithmetic

Carry Lookahead Adder



- **Maximum gate delay for the carry generation is only 3. The full adders introduce two more gate delays. Worst case path is 5 gate delays.**

Principles of Computer Architecture by M. Murdocca and V. Heuring

Standard Logic Components

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3.5 Combinational Circuits

- Decoders are another important type of combinational circuit.
- Among other things, they are useful in selecting a memory location according a binary value placed on the address lines of a memory bus.
- Address decoders with n inputs can select any of 2^n locations.

This is a block diagram for a decoder.

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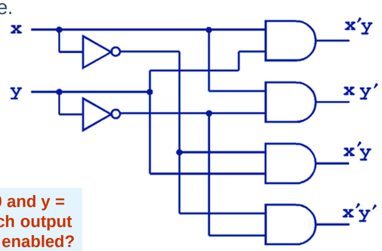
3.5 Combinational Circuits

- This is what a 2-to-4 decoder looks like on the inside.



If x = 0 and y = 1, which output line is enabled?

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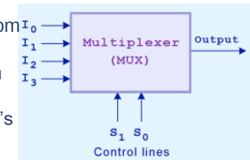
3.5 Combinational Circuits

- A multiplexer does just the opposite of a decoder.
- It selects a single output from several inputs.
- The particular input chosen for output is determined by the value of the multiplexer's control lines.
- To be able to select among *n* inputs, $\log_2 n$ control lines are needed.



This is a block diagram for a multiplexer.

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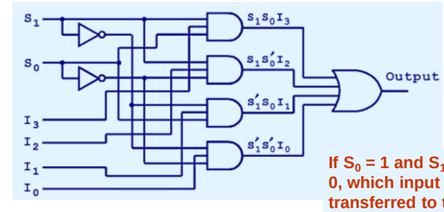
3.5 Combinational Circuits

- This is what a 4-to-1 multiplexer looks like on the inside.



If S_0 = 1 and S_1 = 0, which input is transferred to the output?

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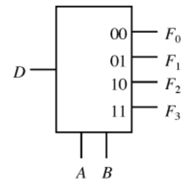
Demultiplexer

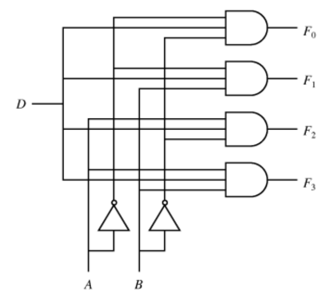


D	A	B	F_0	F_1	F_2	F_3
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

$F_0 = D\overline{A}\,\overline{B}$ $\quad F_2 = DA\overline{B}$

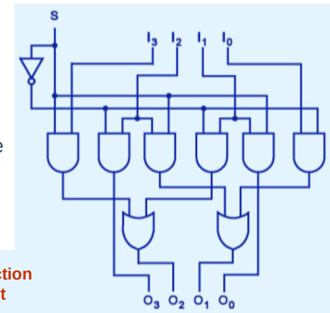
$F_1 = D\overline{A}B$ $\quad F_3 = DAB$

Gate-Level Implementation of DEMUX



3.5 Combinational Circuits

- This shifter moves the bits of a nibble one position to the left or right.



If S = 0, in which direction do the input bits shift?

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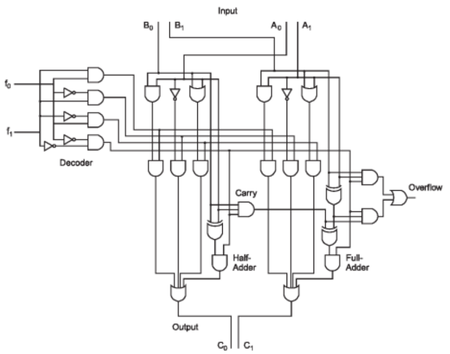

FIGURE 3.17 A Simple Two-Bit ALU

References

- **Materials on semiconductors, PN junction and transistors taken from the HyperPhysics web site:**
  <http://hyperphysics.phy-astr.gsu.edu/hbase/hframe.html>

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