

IA32 Reference Sheet (GNU assembler format)

IA32 instructions

<code>movl Src, Dest</code>	<code>Dest = Src</code>
<code>movsbl Src, Dest</code>	<code>Dest (long) = Src (byte), sign extend</code>
<code>addl Src, Dest</code>	<code>Dest = Dest + Src</code>
<code>subl Src, Dest</code>	<code>Dest = Dest - Src</code>
<code>imull Src, Dest</code>	<code>Dest = Dest * Src</code>
<code>sall Src, Dest</code>	<code>Dest = Dest << Src</code>
<code>sarl Src, Dest</code>	<code>Dest = Dest >> Src</code> arithmetic shift
<code>shrl Src, Dest</code>	<code>Dest = Dest >> Src</code> logical shift
<code>xorl Src, Dest</code>	<code>Dest = Dest ^ Src</code>
<code>andl Src, Dest</code>	<code>Dest = Dest & Src</code>
<code>orl Src, Dest</code>	<code>Dest = Dest Src</code>
<code>incl Dest</code>	<code>Dest = Dest + 1</code>
<code>decl Dest</code>	<code>Dest = Dest - 1</code>
<code>negl Dest</code>	<code>Dest = - Dest</code>
<code>notl Dest</code>	<code>Dest = ~ Dest</code>
<code>leal Src, Dest</code>	<code>Dest = address of Src</code>
<code>cmpl Src2, Src1</code>	Sets CCs <code>Src1 - Src2</code>
<code>testl Src2, Src1</code>	Sets CCs <code>Src1 & Src2</code>
<code>jmp label</code>	jump
<code>je label</code>	jump equal
<code>jne label</code>	jump not equal
<code>js label</code>	jump negative
<code>jns label</code>	jump non-negative
<code>jg label</code>	jump greater (signed)
<code>jge label</code>	jump greater or equal (signed)
<code>jl label</code>	jump less (signed)
<code>jle label</code>	jump less or equal (signed)
<code>ja label</code>	jump above (unsigned)
<code>jb label</code>	jump below (unsigned)
<code>push Src</code>	<code>%esp = %esp - 4,</code> <code>Mem[%esp] = Src</code>
<code>pop Dest</code>	<code>Dest = Mem[%esp],</code> <code>%esp = %esp + 4</code>
<code>call label</code>	push address of next instruction, <code>jmp label</code>
<code>ret</code>	<code>%eip = Mem[%esp],</code> <code>%esp = %esp + 4</code>

Addressing modes

• Immediate

`$val Val`
`val:` constant integer value
`movl $17, %eax`

• Normal

`(R) Mem[Reg[R]]`
`R:` register R specifies memory address
`movl (%ecx), %eax`

• Displacement

`D(R) Mem[Reg[R]+D]`
`R:` register specifies start of memory region
`D:` constant displacement D specifies offset
`movl 8(%ebp), %edx`

• Indexed

`D(Rb, Ri, S) Mem[Reg[Rb]+S*Reg[Ri]+D]`
`D:` constant displacement 1, 2, or 4 bytes
`Rb:` base register: any of 8 integer registers
`Ri:` index register: any, except `%esp`
`S:` scale: 1, 2, 4, or 8
`movl 0x100(%ecx, %eax, 4), %edx`

Instruction suffixes

`b` byte
`w` word (2 bytes)
`l` long (4 bytes)

Condition codes

CF Carry Flag
ZF Zero Flag
SF Sign Flag
OF Overflow Flag

Registers

<code>%eax</code>
<code>%ecx</code>
<code>%edx</code>
<code>%ebx</code>
<code>%esi</code>
<code>%edi</code>
<code>%esp</code>
<code>%ebp</code>